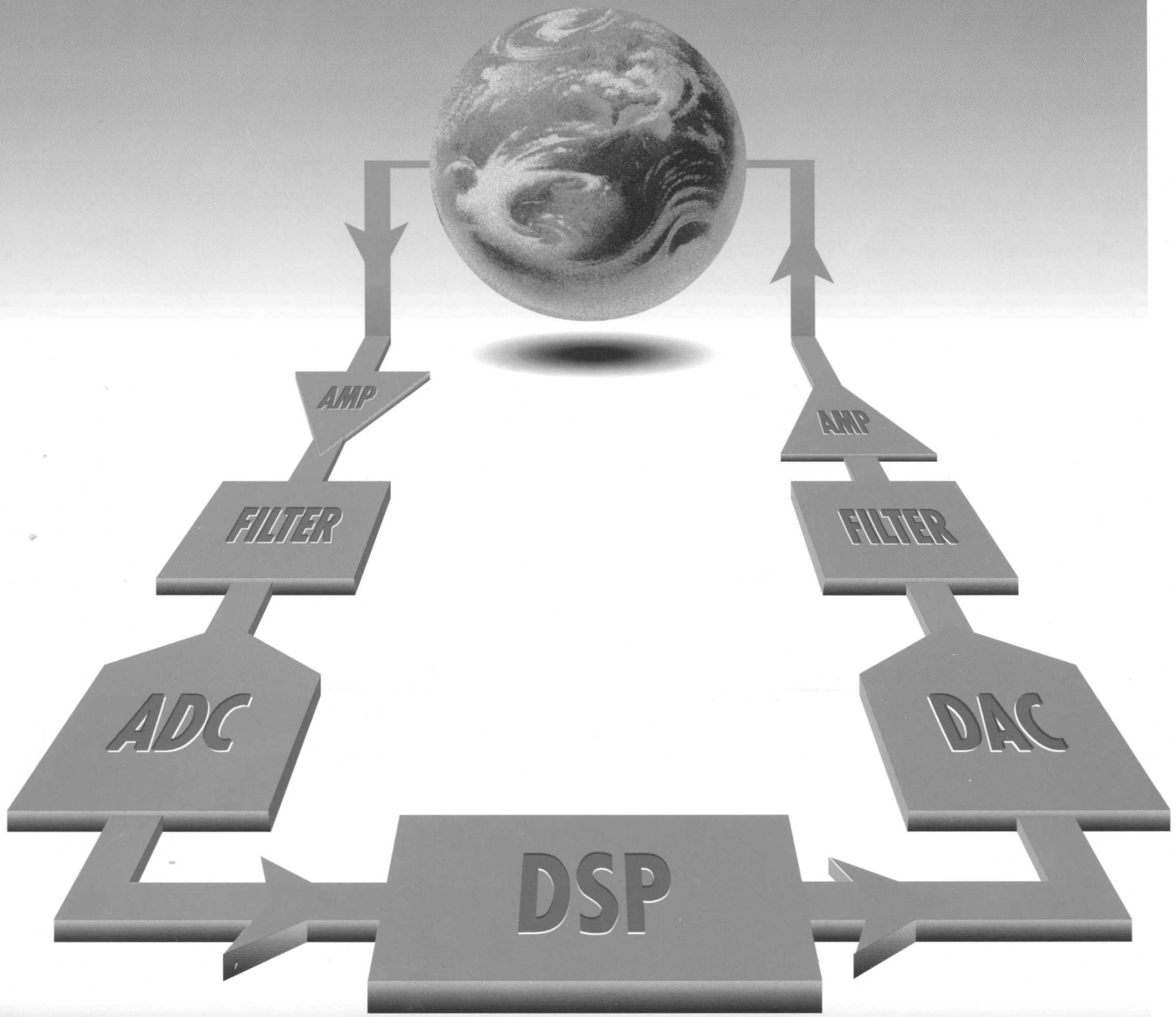
BURR-BROWN®

Applications Seminar



Noise Gain vs Frequency Plot

$$f_1 = \frac{1}{2\pi(R_1 \| R_2)C_1 + C_A + C_2 + C_{R_2}}$$

$$f_2 = \frac{1}{2\pi R_2 (C_2 + C_{R_2})}$$

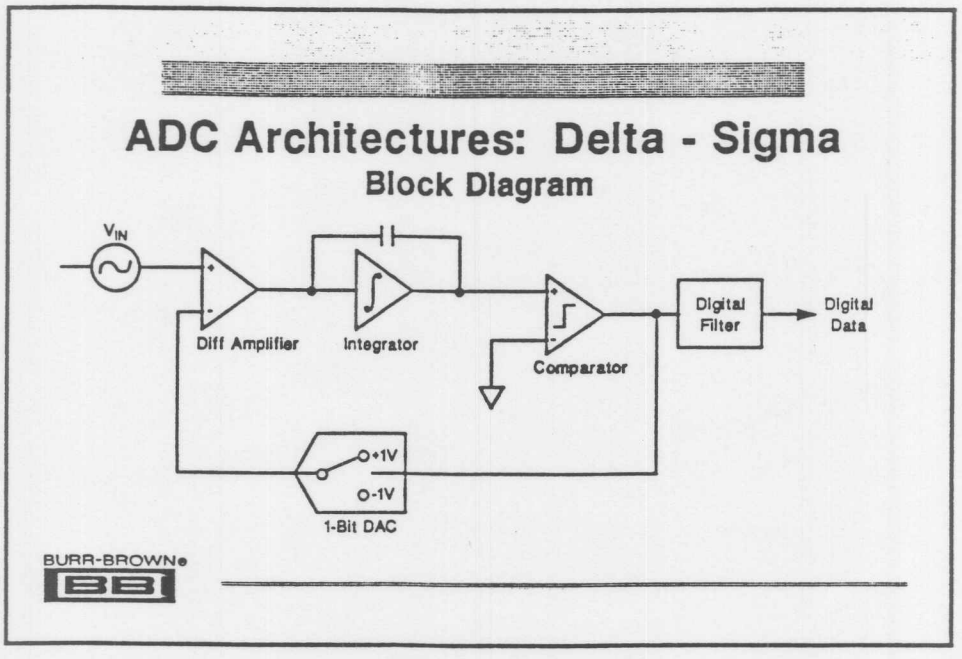
$$f_{A_{OL}} = \sqrt{\frac{f_U}{2\pi R_2 (C_1 + C_A)}}$$

Noise Calculation Example

$$V_{OUT}(\text{Noise}) = \sqrt{e_1^2 + e_2^2 + e_3^2 + e_4^2 + e_5^2 + e_{R_2}^2 + e_I^2}$$

$$= \sqrt{0.267^2 + 0.21^2 + 15.1^2 + 125.5^2 + 96.9^2 + 64.9^2 + 16.9^2}\ \mu V_{RMS}$$

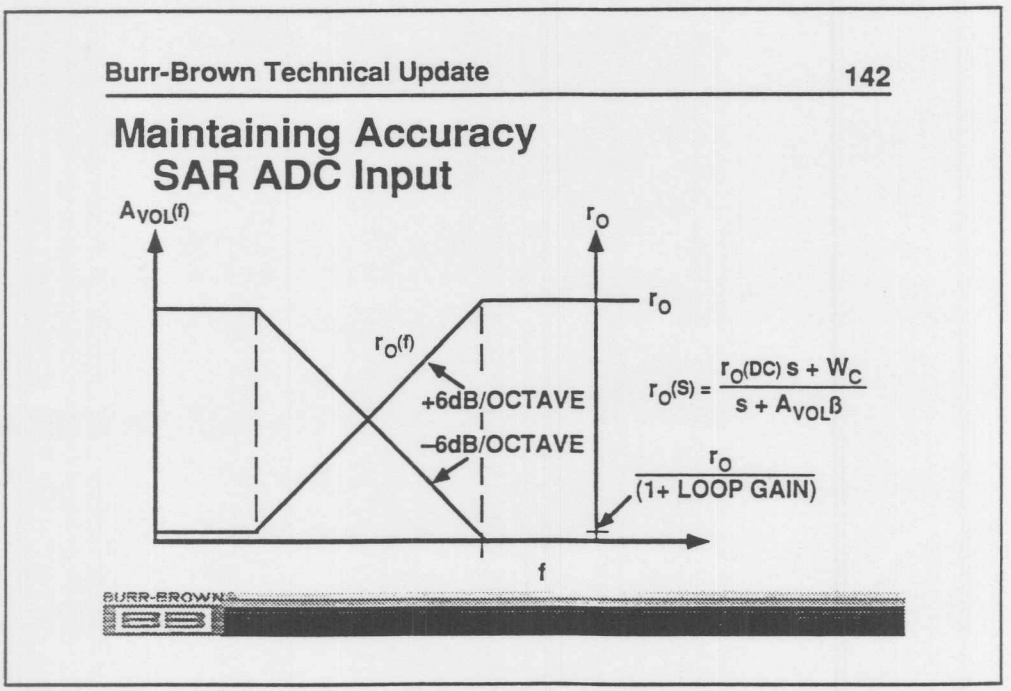
$$= 173 \mu V_{RMS}$$



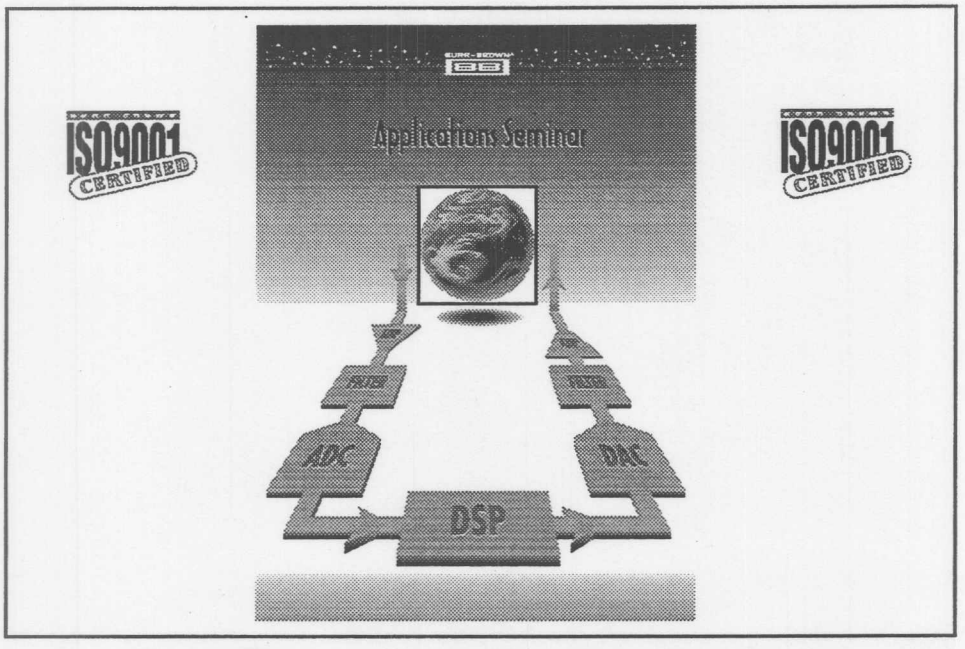
Delta-Sigma ADC Block Diagram

The block diagram above represents a one-bit delta-sigma ADC in the time domain. The input signal is sent into a difference amp, where the output of the one-bit DAC is subtracted from it. This difference is then integrated and sent to the one-bit ADC (comparator as shown above). The output of the ADC then feeds the DAC, and the conversion process starts again. The bitstream is then integrated over a certain period by the digital filter, which results in an n bit output.

The digital filter acts as a noise shaper by moving the large quantization noise into the stopband, closer to Fs. However, in a one-bit delta-sigma ADC, the demands placed on the digital filter to produce good SNR are tremendous. An improvement can be seen in SNR by using a multi-bit quantizer. This method is used in Burr-Brown's PCM1760, which employs a four-bit flash ADC as well as a 4-bit DAC. These multi-bit devices are laser-trimmed to 18-bit accuracy.



An op amp's output impedance increases as the loop gain decreases, as shown here. This can cause the output impedance, $r_O(s)$, to be significant at high frequencies. Thus, it's important to choose an op amp which has a very low output impedance, and has wide bandwidth so that the low output impedance is preserved at high frequency.

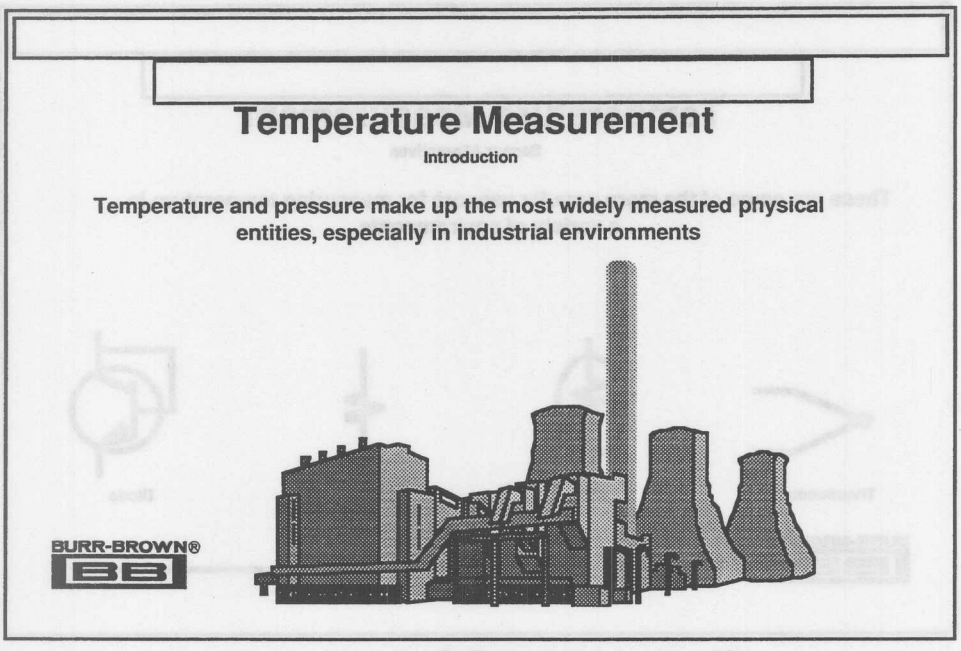


Burr-Brown Application Seminar

Conditioning You To Precision Analog

Welcome to Burr-Brown's Applications Seminar. We will be covering problems found in analog system design, and some component based solutions to these problems. Primarily, we will look at problems related to precision, accuracy, noise and speed.

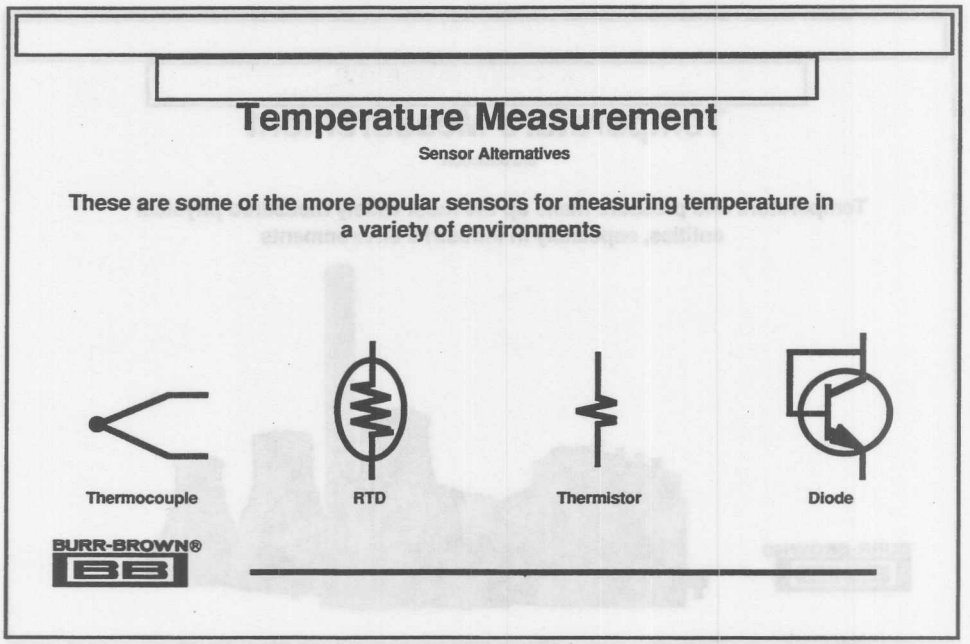
In the real world, we need to acquire signals from some physical entity for subsequent analysis. These signals may consist of temperature, pressure, light, ac signals, etc... As a system designer, you are faced with acquiring these signals and processing them with a minimal amount of interference from your processing components. Burr-Brown specializes in component solutions emphasizing low noise, high accuracy and high speed. In this seminar, we will discuss the problems associated with analog signal conditioning, digitization and output, and we will show you simple component solutions to these problems. Prepare to be *conditioned to precision analog*.



Temperature Measurement

Introduction

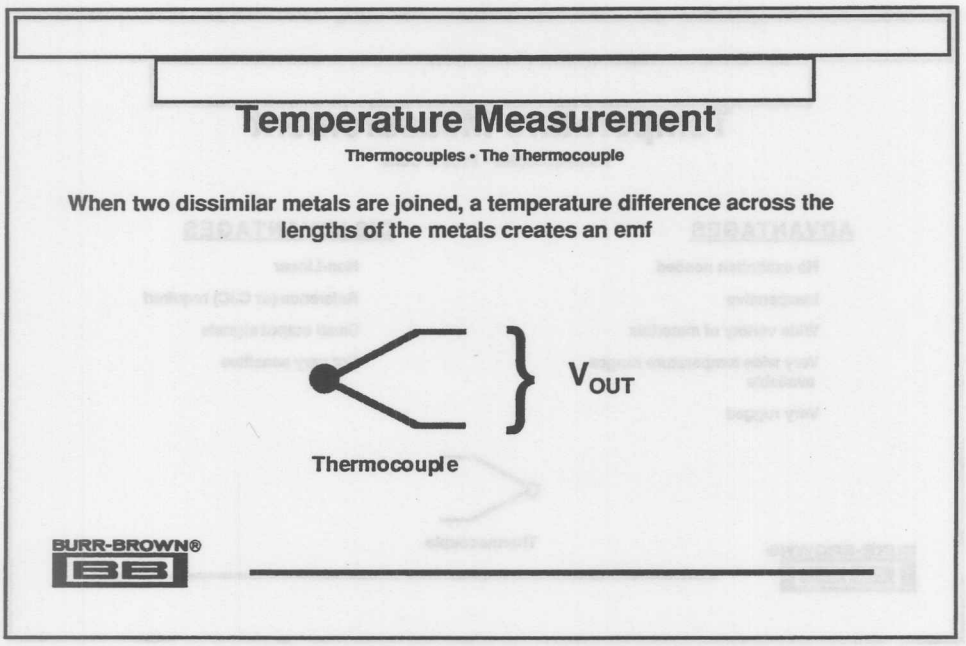
In a wide variety of environments and systems, many different physical properties are measured. Some of these properties are temperature, pressure, light, flow, level, etc... Their values may just be monitored, or decisions may need to be made in response to changing data as in a process control system. However, probably the most commonly measured physical property is temperature.



Temperature Measurement

Sensor Alternatives

Depending on temperature deltas, accuracy desired, and budget considerations, a wide variety of temperature sensors are available. Some of the most popular types of sensors are the thermocouple, RTD, thermistor, and diode. And within each of these sensor families exist a variety of "types". For example, a few of the thermocouple types are: J, K, R, etc...; RTDs are available in a variety of materials, several of which are available with different resistances at 0°C. Also, any generic, garden variety, diode can be used for temperature sensors, as well as diodes optimized for this function such as Motorola's MTS100 series.

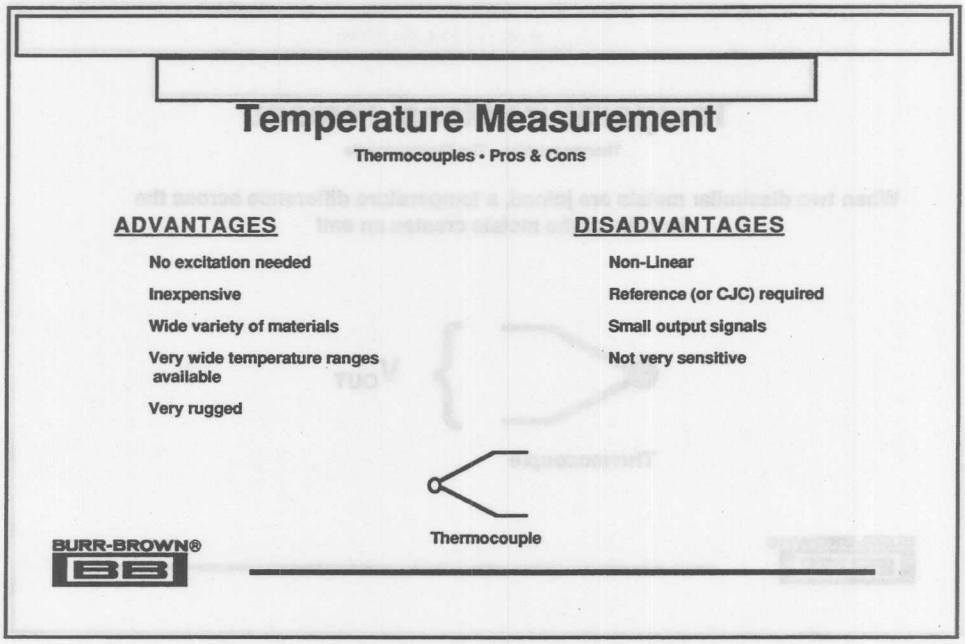


Temperature Measurement

Thermocouples • The Thermocouple

When two dissimilar metals are connected together and there is a temperature difference from one end of the metals to the other end, there is an emf, or voltage created. The voltage produced under these conditions is known as the Seebeck emf. This voltage is a function of the temperature gradient, or difference, across the length of the metals, and the materials used. This is a phenomena associated with joining any dissimilar metals, and is referred to as a thermocouple.

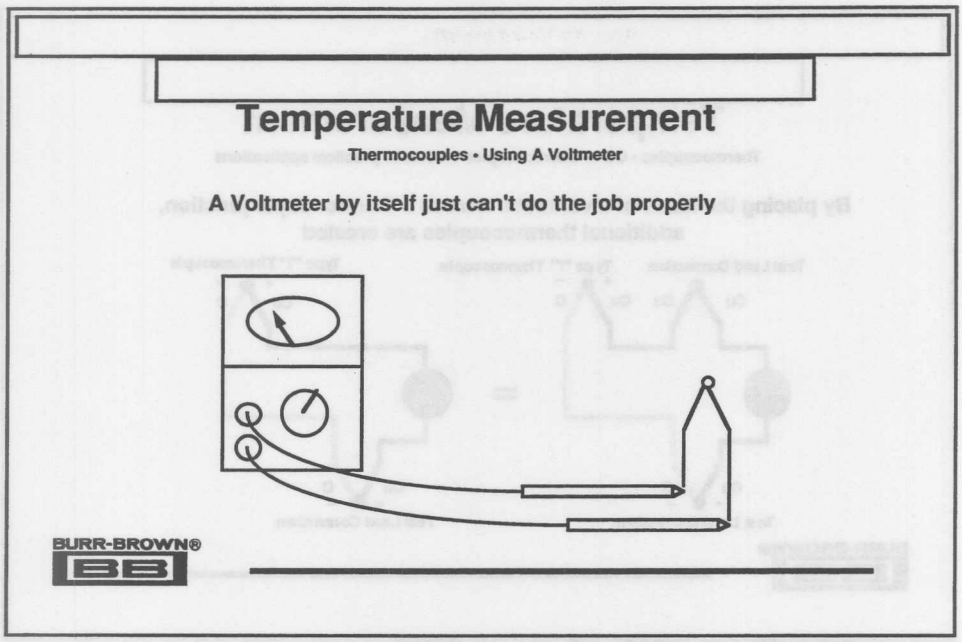
One commonly misunderstood fact is that the voltage is not created at the "weld" of the dissimilar metals, but all along the thermocouple itself. For example, if an entire thermocouple was placed in an environment such that all portions of the thermocouple are at the same temperature, there is no voltage created!



Temperature Measurement

Thermocouples • Pros & Cons

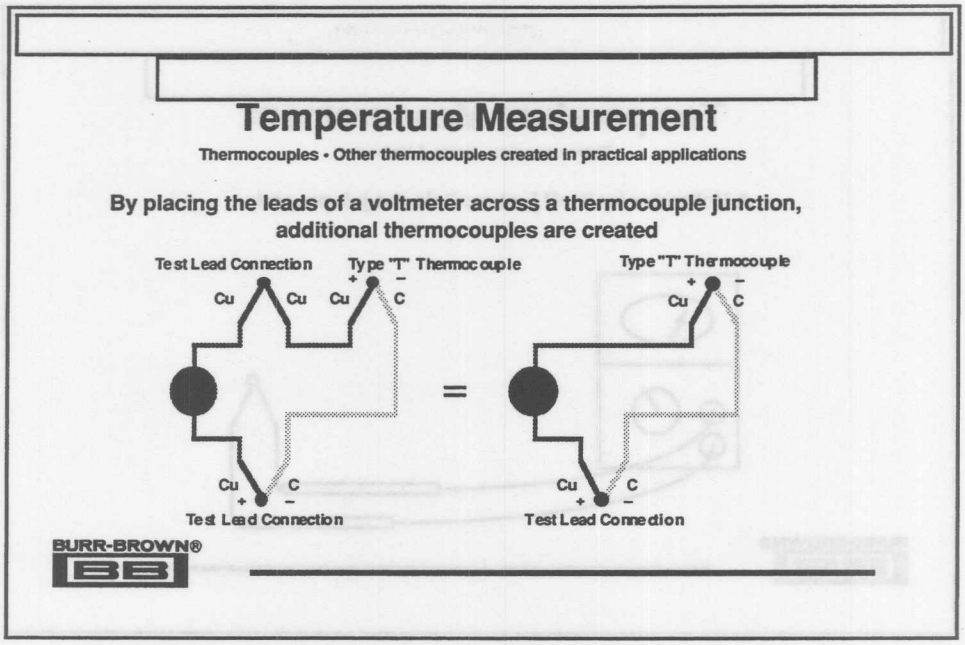
Thermocouples are typically low impedance, voltage output devices which offer some advantages over other temperature sensing devices. They are very rugged, can be used in very harsh environments and can be mechanically attached to devices with hardware. They can be made very small in order to reduce their thermal time constants, and they operate over very wide temperature ranges (Type "S" is useful over a temperature range of about 0°C to 1700°C). Due to the nature of the thermocouple no excitation or biasing is necessary, and they are also one of the least expensive temperature sensing devices available. On the other hand, thermocouple outputs are very small nonlinear signals, which require some type of known reference or compensation -- and they're not very sensitive.



Temperature Measurement

Thermocouples • Using A Voltmeter

Now that we know exactly what it is we are measuring, it would be nice to think that we could place a voltmeter across a thermocouple in order to measure the Seebeck emf. However, this causes adverse effects due to the leads of the measurement thermocouple and the voltmeter providing other thermocouple junctions.

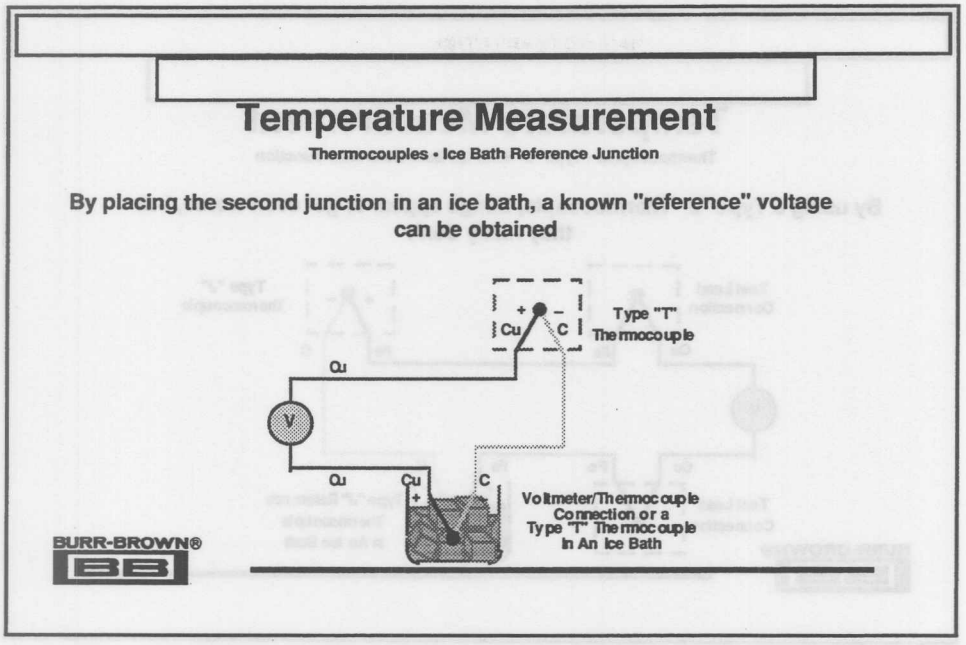


Temperature Measurement

Thermocouples • Other thermocouples created in practical applications

In this example, a Type "T" thermocouple has been used. This thermocouple has one lead of copper and another of constantan, and is useful over a temperature range of about -160°C to 400°C. However, where the thermocouple's constantan lead connects with the copper lead of the voltmeter, another type "T" thermocouple has been developed. Where the copper lead of the thermocouple connects with the copper lead of the volt meter, no thermocouple junction exists due to the similar metals.

Following the polarity of the circuit, you can see that the voltage that is read on the voltmeter, is representative of the temperature of the thermocouple minus the temperature of the test lead connection.

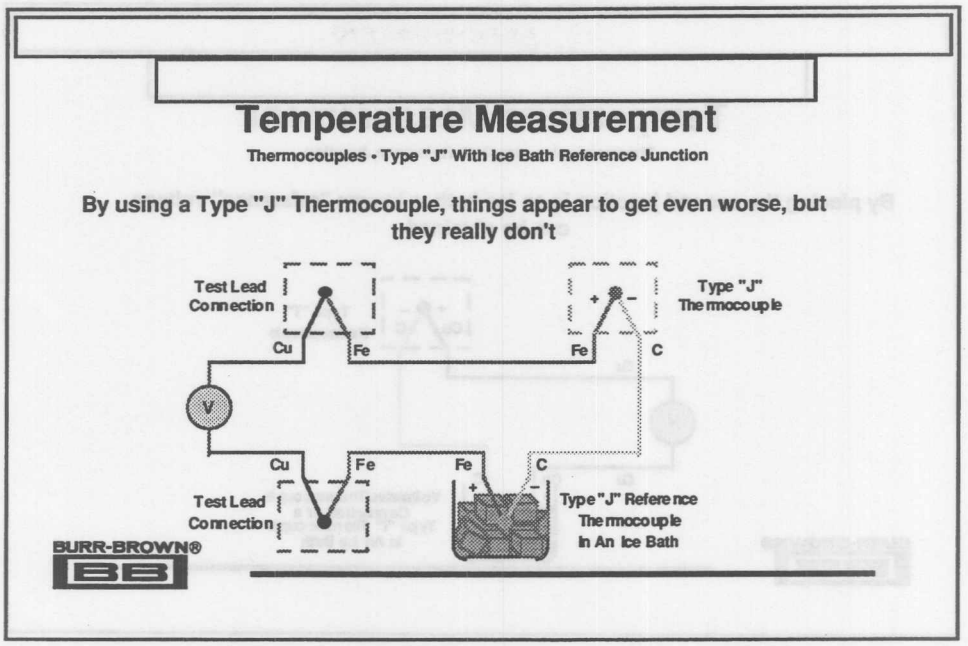


Temperature Measurement

Thermocouples • Ice Bath Reference Junction

If the connection of the copper voltmeter lead and the constantan thermocouple lead is placed in an ice bath, or if the constantan connection to the voltmeter is opened and another type "T" thermocouple is inserted into this connection, the new thermocouple can be subjected to a known temperature providing a known offset or "reference". When placed into an ice bath, the resulting temperature of a thermocouple is forced to 0°C, creating a known EMF.

However, it is not practical in most applications to have one of your electrical connections in an ice bath for long periods of time! Therefore, we will be discussing other types of reference circuits in just a bit.

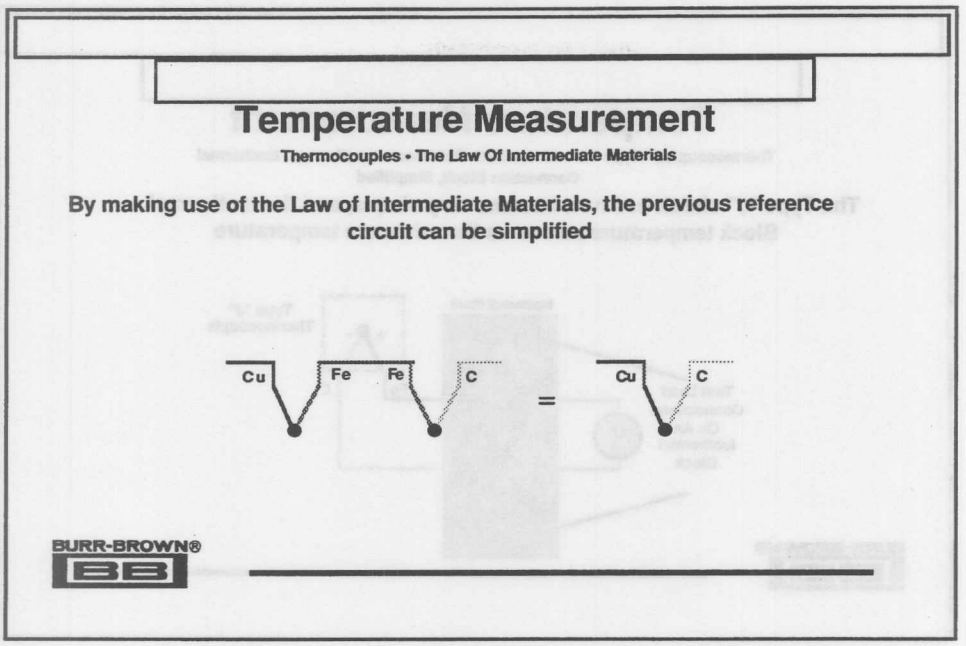


Temperature Measurement

Thermocouples • Type "J" With Ice Bath Reference Junction

By using a Type "J" thermocouple to measure the 0°C to 750°C range, things appear to get even more complicated with voltmeter connections. The Type "J" thermocouple is constructed of Iron and Constantan, so neither of the thermocouple leads are made of the same material as the voltmeter leads. Not only do we need the reference thermocouple, shown here in a 0°C ice bath (remember, I'm going to get away from the ice bath later), but there is also a voltage created due to the iron thermocouple lead joining the copper voltmeter lead

However, as long as these two connection points are kept at the same temperature, they should not introduce any error as the voltages created cancel each other.

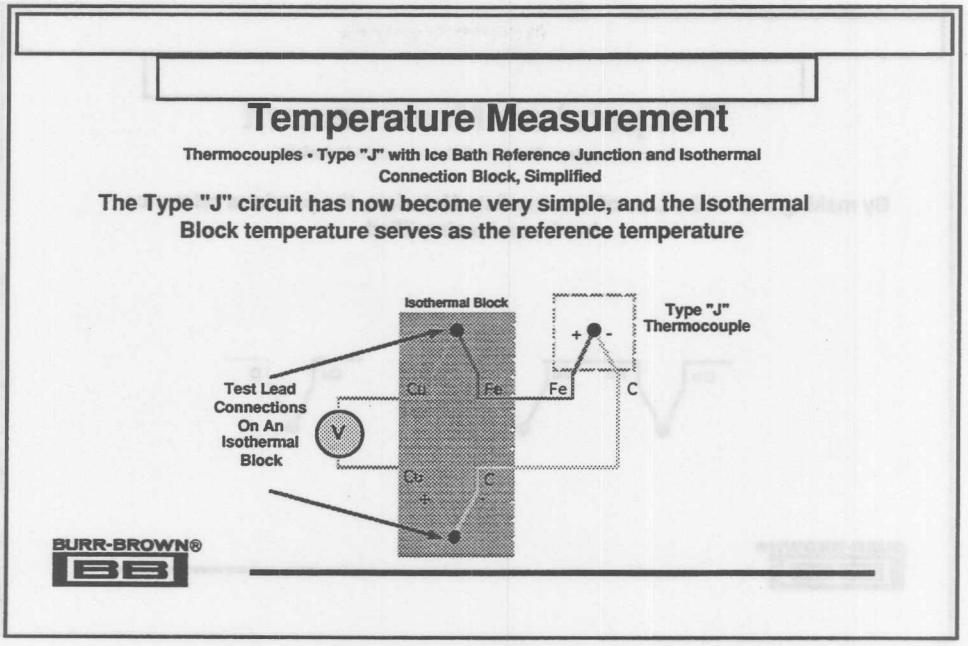


Temperature Measurement

Thermocouples • The Law Of Intermediate Materials

By using the law of intermediate materials, the "reference" part of the circuit can be simplified somewhat. According to Omega (a well known sensor manufacturer): "...a third metal (in this case, iron) inserted between the two dissimilar metals of a thermocouple junction will have no effect upon the output voltage as long as the two junctions formed by the additional metal are at the same temperature"[1]. Let's see what this does to the previous circuit...

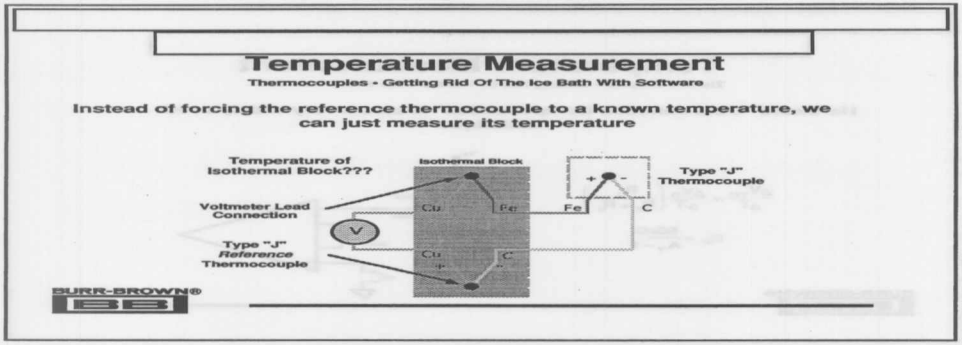
1) OMEGA Complete Temperature Measurement Handbook and Encyclopedia, vol #28, p Z-15, Omega Engineering Incorporated, Stamford, Connecticut, ©1992



Temperature Measurement

Thermocouples • Type "J" with Ice Bath Reference Junction and Isothermal Connection Block, Simplified

By effectively moving the reference thermocouple to the isothermal block, the effects of the copper voltmeter lead/iron thermocouple connection have been cancelled. Now the circuit output is a function of temperature at the measurement thermocouple with respect to the temperature of the isothermal block.

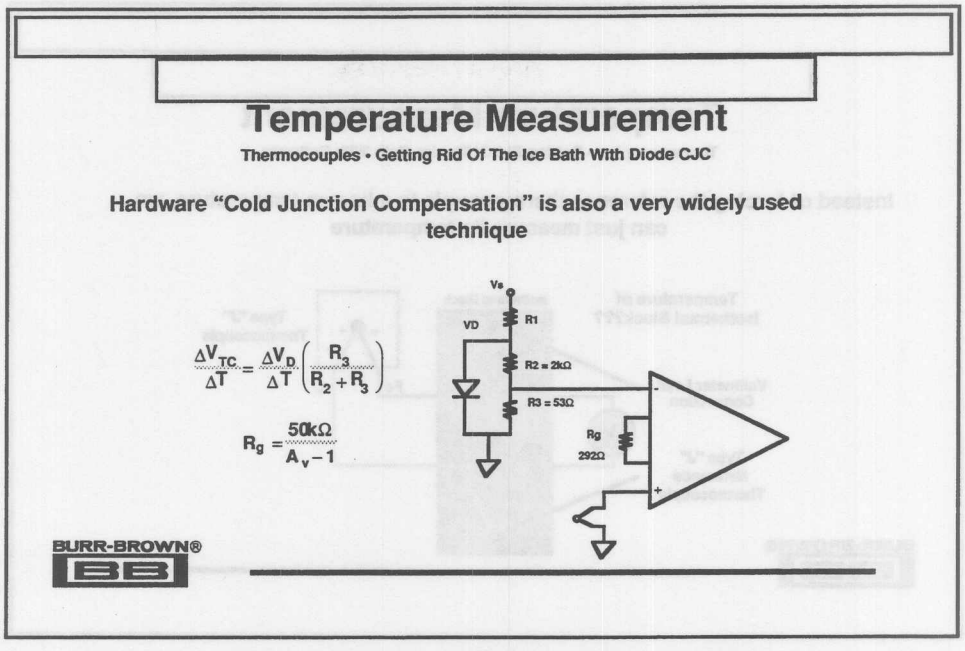


Temperature Measurement

Thermocouples • Getting Rid Of The Ice Bath With Software

As stated earlier, having a reference thermocouple in an ice bath just isn't practical most of the time in "real world" applications. We will now address other reference means.

The previous slide, which had the reference thermocouple on the isothermal block, showed that the circuit output is a function of the measurement thermocouple temperature minus the isothermal block temperature. Now all we need to know is the temperature of the isothermal block. There are a variety of means to accomplish this, but all of them require an absolute temperature sensor (remember that a thermocouple's output is a function of the temperature difference across it). Suitable alternatives for this might consist of RTDs, thermistors, or diodes (these sensors will be covered shortly).

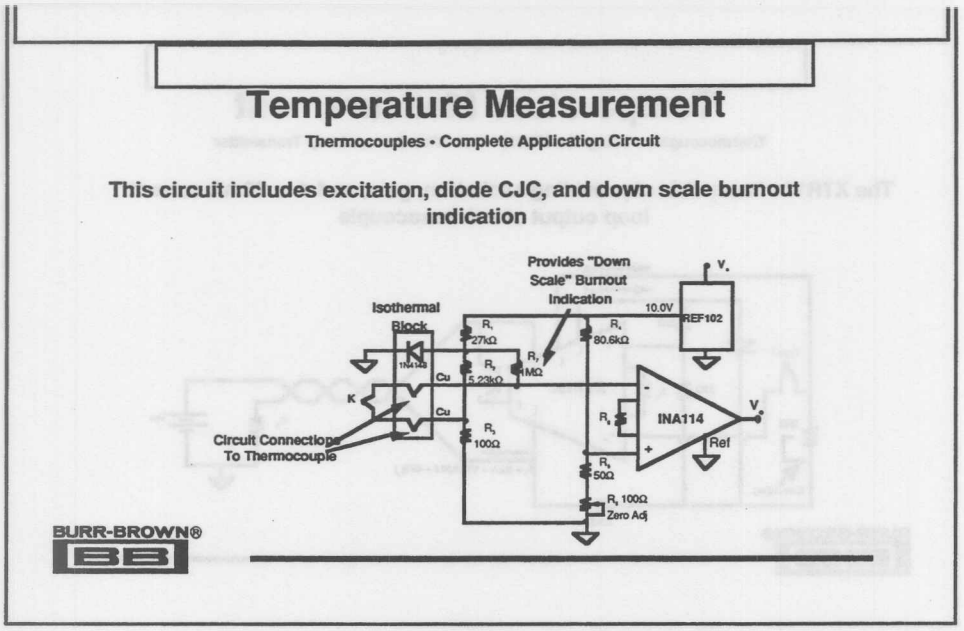


Temperature Measurement

Thermocouples • Getting Rid Of The Ice Bath With Diode CJC

In this example, a Type "J" thermocouple is used to measure process temperatures from 0°C to +1000°C, and a diode is used to provide the reference circuit. This is accomplished by supplying a voltage to the IA's negative input which is equal to that normally produced by the thermocouple with it's "cold junction" at ambient. At a typical ambient of +25°C this is 1.277mV (obtained from standard thermocouple tables with reference junction of 0°C). The voltage across the thermocouple will span about 58mV as the thermocouple measures across the 0°C to 1000°C temperature range, leading to a gain setting resistor value of approximately 292Ω. At +25°C, the voltage across the diode is approximately 0.6V, and $\Delta V_D/\Delta T$ is equal to -2mV/°C. The divider (R_2 & R_3) values are selected so that the tempco $\Delta V_D/\Delta T$ equals the tempco of the thermocouple at the reference temperature. At +25°C this is approximately 51.7µV/°C.

Therefore, $\Delta V_{TC}/\Delta T = \Delta V_D/\Delta T(R_3/(R_2+R_3))$, or $51.7\mu V/°C = 2mV/°C(R_3(R_2+R_3))$. R_2 was arbitrarily chosen to be 2kΩ which is much larger than the resistance of the diode. Solving for R3 yields 53Ω.

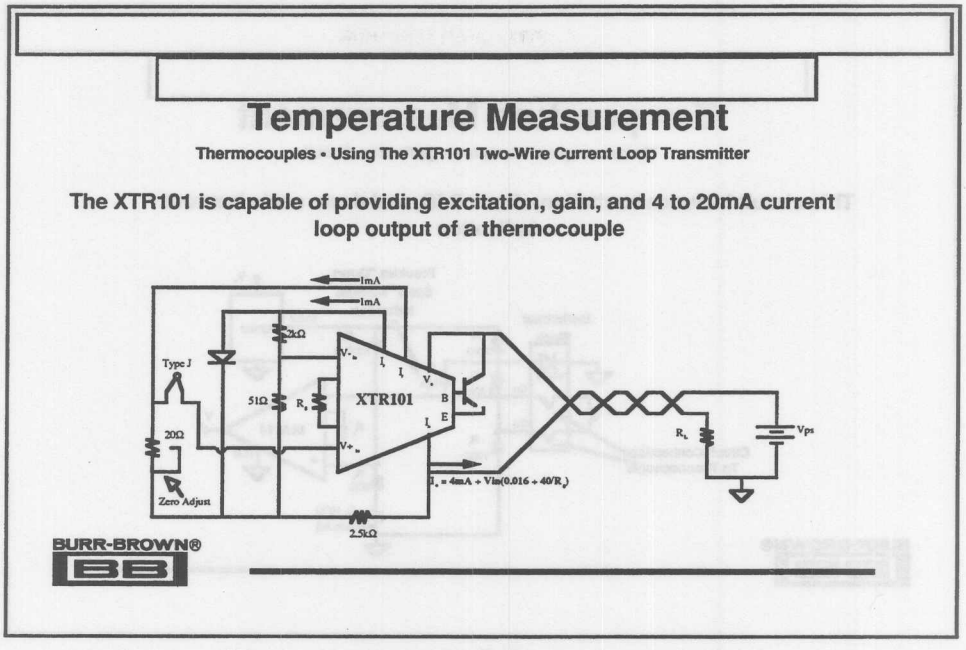


Temperature Measurement

Thermocouples • Complete Application Circuit

This circuit utilizes Burr-Brown's REF102 for exciting a Type "K" thermocouple, a 1N4148 diode used for cold junction compensation, and the zero reference circuit, while the INA114 is used to amplify the difference input. The 1MΩ resistor provides a "down scale" burnout indication for thermocouple open circuit conditions (open circuits are the most common failure mode for thermocouples). The table below can be used for values when using other thermocouple types.

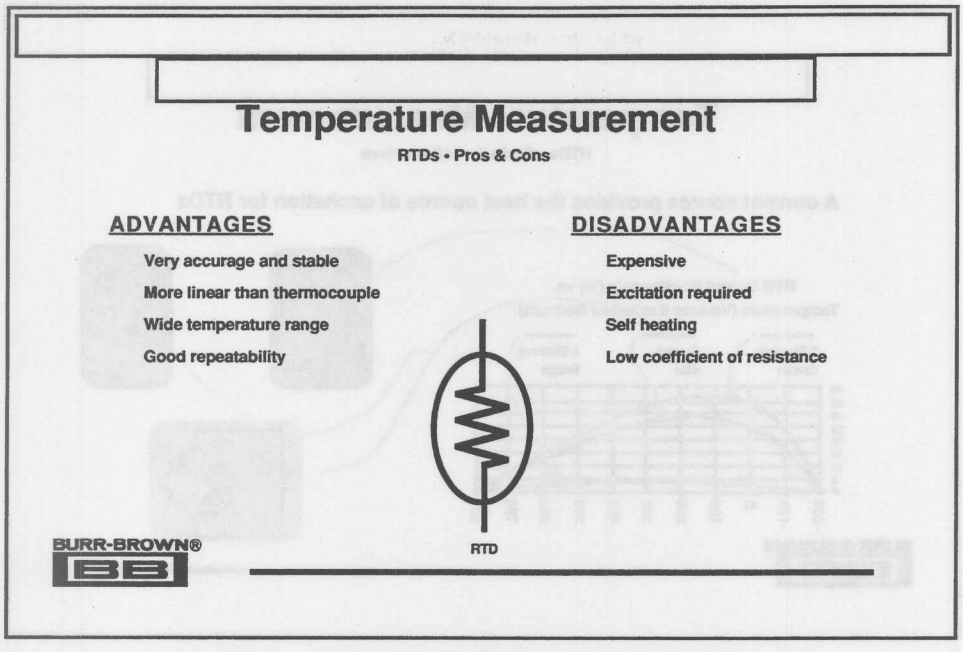
ISA Type	Material	Seebeck Coefficient (μV/°C)	R_2 (R_3 = 100Ω)	R_4 ($R_5 + R_6$ = 100Ω)
E	Chromel Constantan	58.5	3.48kΩ	56.2kΩ
J	Iron/Constantan	50.2	4.12kΩ	64.9kΩ
K	Chromel/Alumel	39.4	5.23kΩ	80.6kΩ
T	Copper/Constantan	38.0	5.49kΩ	84.5kΩ



Temperature Measurement

Thermocouples • Using The XTR101 Two-Wire Current Loop Transmitter

A lot of thermocouples are located somewhat remote to the electronics, and this typically causes problems when trying to monitor voltages great distances away. The voltage signal which is transmitted is affected by noise and I•R drops all along the transmission line. The XTR101 shown here converts the low level thermocouple output into a 4-20mA current loop signal. This signal becomes immune to the noise and/or I•R drops which commonly afflict measurements. The 20Ω potentiometer has been used here to calibrate the system at the minimum temperature of interest.

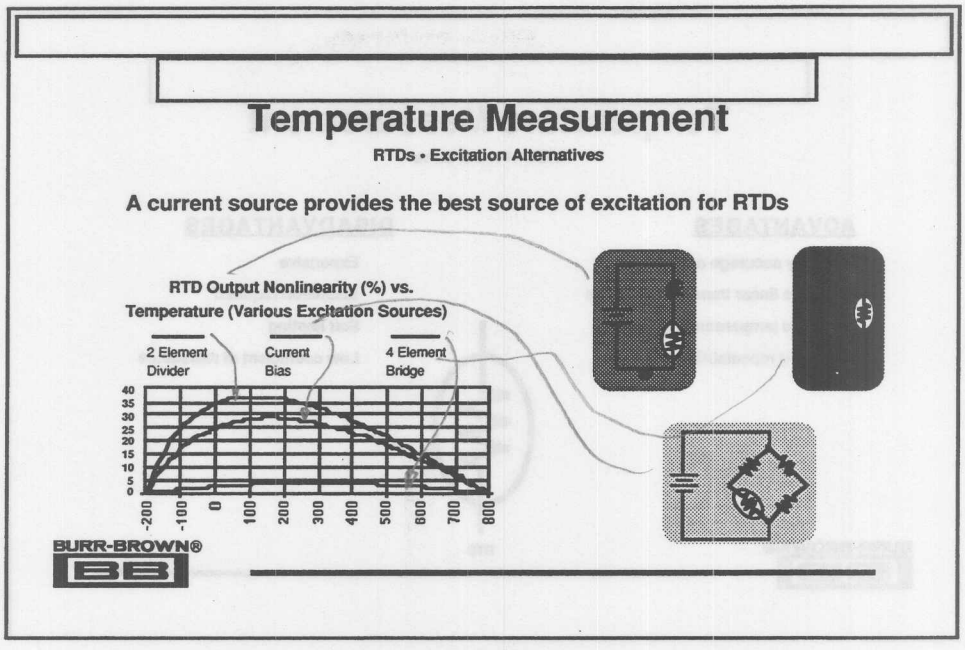


Temperature Measurement

RTDs • Pros & Cons

RTDs are available in a variety of materials, but platinum seems to offer advantages over other metals. Its high resistivity (59Ω/circular mil foot) leads to smaller physical sizes than if nickel or other metals had been used, and this creates smaller thermal time constants. Platinum is also usable over a wider temperature range than nickel, and is less susceptible to environmental contamination. Platinum RTDs (as well as those constructed with other materials) are also available with various values of R_0 (resistance at 0°C). For the reasons previously stated, platinum RTDs (with R_0 = 100Ω) will be the subject of this material. RTDs offer several advantages over other temperature sensing devices. Primarily, they are very accurate and stable, their outputs are more linear than thermocouple or diode sensors, they have a fairly wide temperature range (not as wide as some thermocouples), and their repeatability over time is very good. However, they require excitation which leads to self heating, and they are relatively expensive when compared to thermocouples.

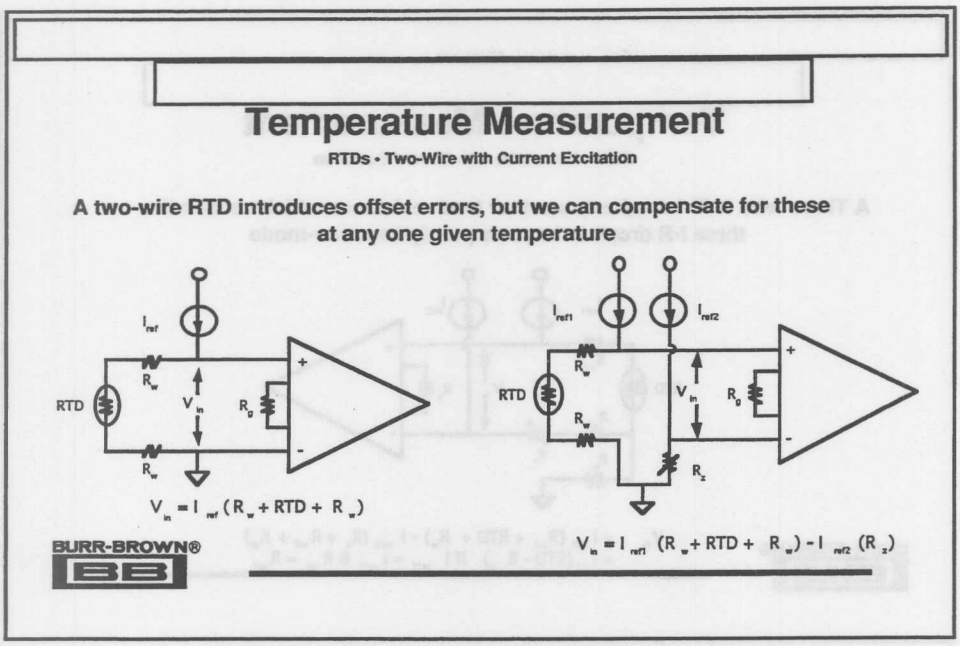
To reduce self heating turn on to read with AC then turn off.



Temperature Measurement

RTDs • Excitation Alternatives

When a voltage is used to bias an RTD in a simple 1/2 bridge (2 element resistive divider), tremendous nonlinearities occur. This is because the current through, and the voltage across, are both changing as the resistance of the RTD changes. By placing the RTD in a 4 element "Wheatstone" bridge, the nonlinearity is improved over the resistive divider, but it is still no where near optimal. Biasing the RTD with a fixed current source removes all nonlinearities associated with the divider action, and only the inherent nonlinearity of the RTD exists in the output.



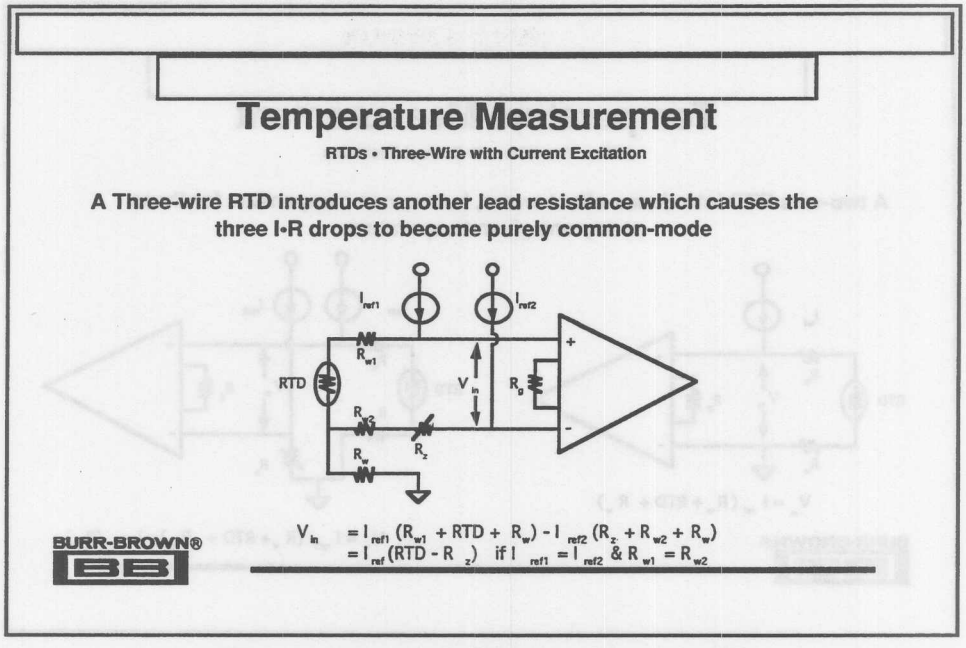
Temperature Measurement

RTDs • Two-Wire with Current Excitation

Now that we've decided that a current source is the best means for exciting an RTD, let's look at some of the other errors associated with the system. The first circuit shown here is the simplest implementation of a temperature measurement system using an RTD. A current source, I_{ref} is used to excite the two-wire RTD, and the instrumentation amplifier output is proportional to the temperature. However, there will always be an output from the amplifier, even when the temperature of the RTD is well below its minimum specified temperature. Also, a lot of RTDs are located somewhat remote to the electronics, causing any current that flows through the lines to the RTD to create a voltage drop due to the line resistances. "The total lead wire resistance should be less than one percent of the sensor resistance"[2].

The second circuit shows a more practical implementation of the two-wire RTD. A second current source (Burr-Brown's REF200 - Dual Current Source might be good here) is used to develop a voltage across a "zero" setting resistor, R_z. This resistor allows for the output of the amplifier to be zero at the minimum temperature of interest, regardless of the magnitude of the line resistances. However, the line resistances are temperature dependent which might cause errors in high gain systems which measure small temperature deltas, but the magnitude of these errors is usually insignificant.

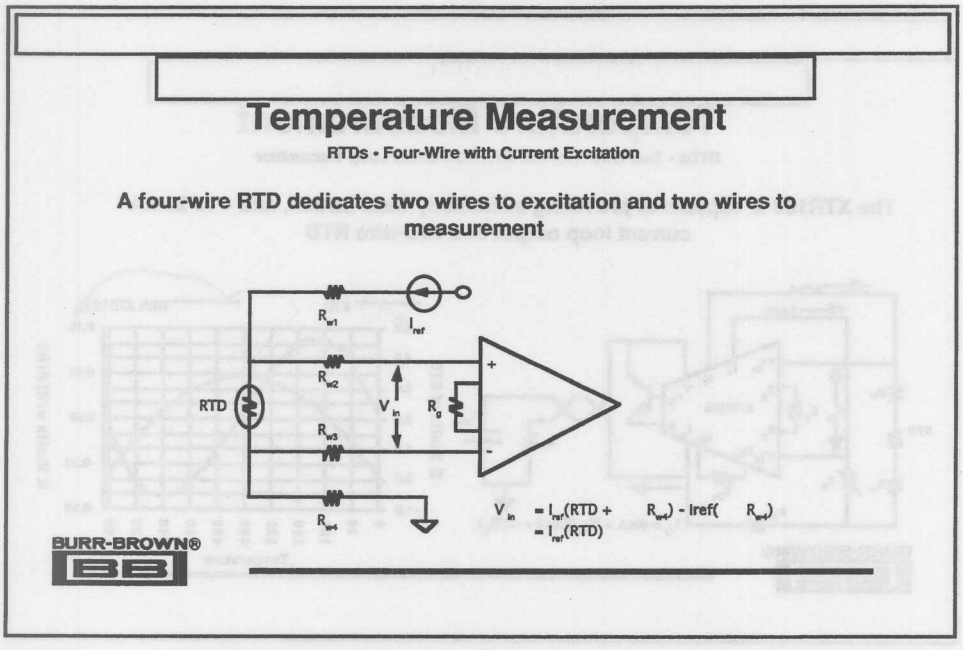
2) James W. Dally, William F. Riley, Kenneth G. McConnell: Instrumentation For Engineering Measurements, p407, John Wiley & Sons, Inc, New York, ©1984



Temperature Measurement

RTDs • Three-Wire with Current Excitation

The three-wire RTD is perhaps the most popular form of RTD. The third wire provides another resistance which can be used in to make the I•R drops (I_{ref1}•R_{w1} and I_{ref2}•R_{w2}) common mode voltages for the amplifier. For the two I•R drops to be equal, the magnitude of the current sources and the length/material of the leads. When this condition is met, the input to the amplifier is reduced to I_{ref}• RTD. Now the amplifier's output is purely indicative of the temperature of the RTD.

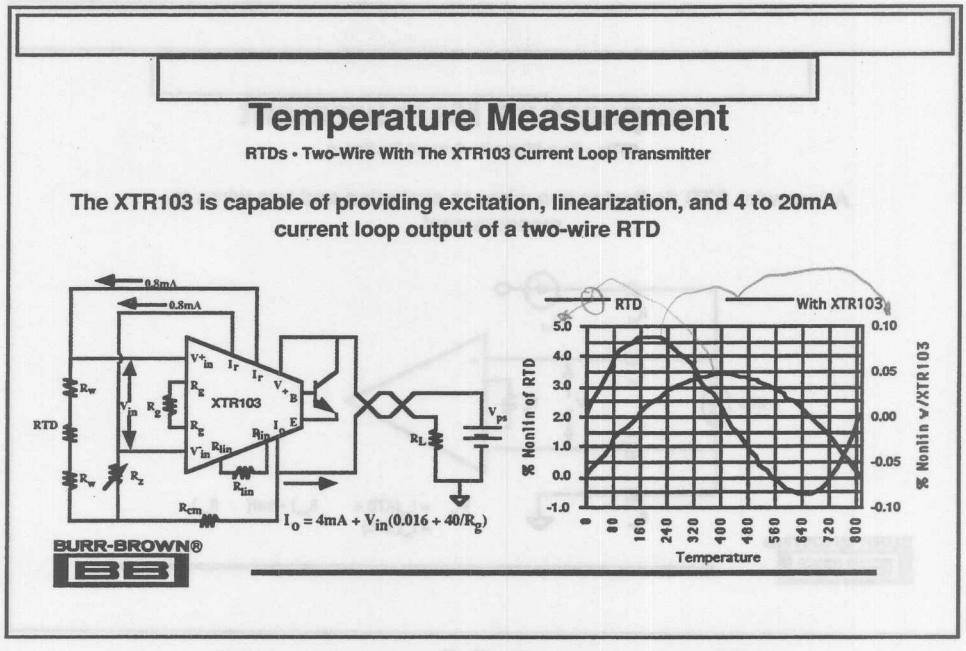


Temperature Measurement

RTDs • Four-Wire with Current Excitation

The four-wire RTD provides the highest precision of any RTD configuration. The reference current is sent through two of the leads, while the signal is measured across two other leads - similar to a force/sense scenario. Due to the high impedance inputs of the instrumentation amplifier, none of the reference current is allowed to flow through R_{w2} and R_{w3} to create the offset seen with the two wire system. The I•R drop due to the reference current and R_{w4} is purely a common mode signal for the amplifier, and rejected by its common mode rejection capabilities.

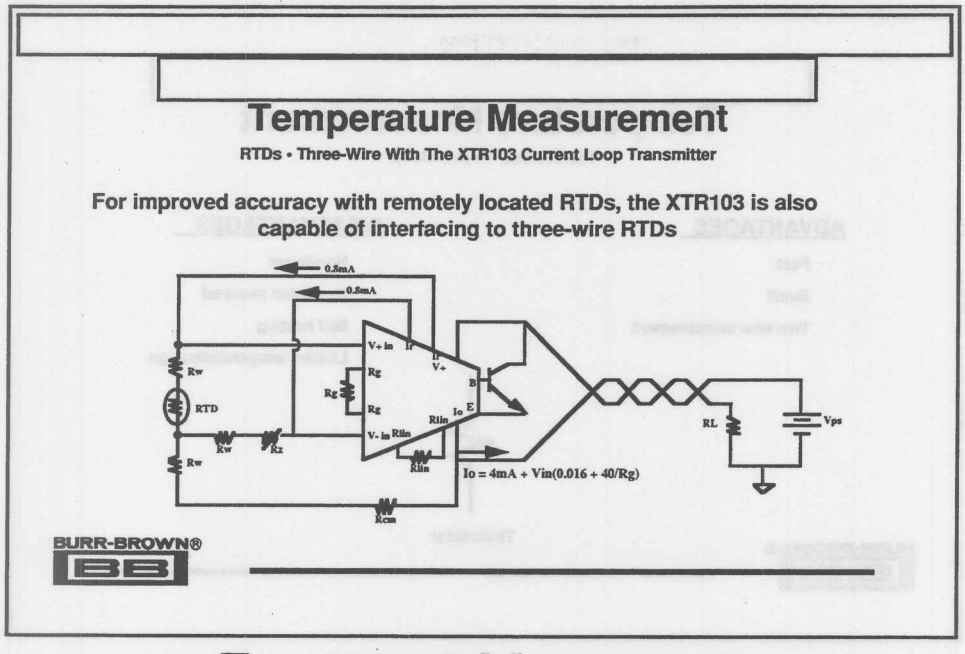
The four-wire system offers no real advantages over the three wire system unless the leads are constructed of different materials, and the three wire system is usually chosen.



Temperature Measurement

RTDs • Two-Wire With The XTR103 Current Loop Transmitter

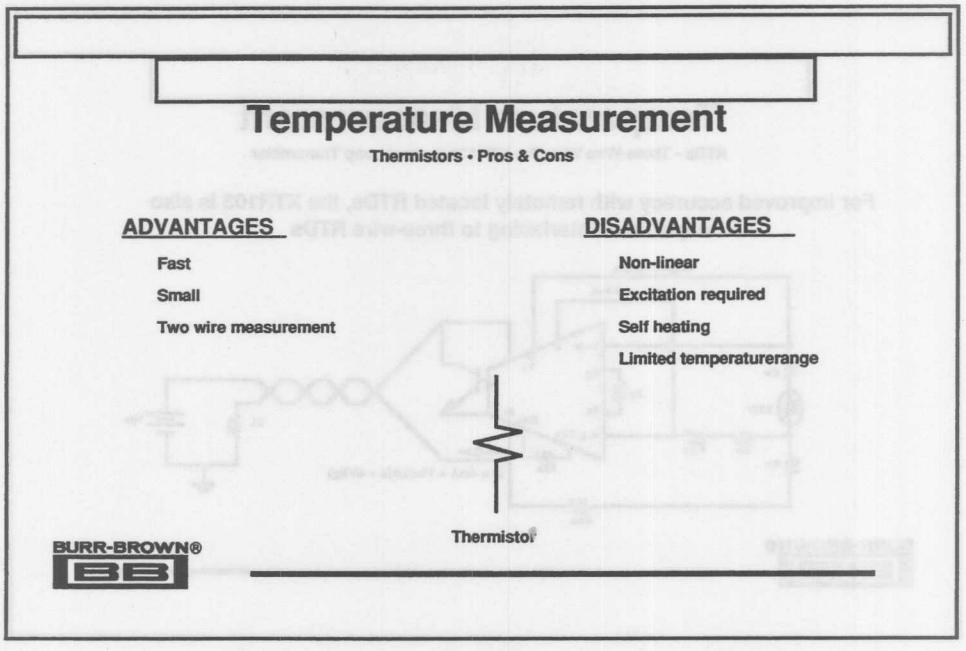
As when we discussed the thermocouple applications, the process temperature being measured is usually located remotely to the electronics. The XTR103 is the answer to remote temperature sensing with RTDs. By providing two 0.8mA current references for RTD and "zero element" biasing, gain, linearization, and 4-20mA current loop output, the XTR103 is a complete solution. Shown here with a two-wire RTD, the XTR103 is capable of reducing the initial nonlinearities of the RTD by a factor of at least 40x.



Temperature Measurement

RTDs • Three-Wire With The XTR103 Current Loop Transmitter

The XTR103 is also capable of interfacing to three-wire RTDs. These are used to negate the I•R drops that are created with the RTD's line resistance reacting with the current source. This configuration turns these voltage drops into common mode voltages which are rejected by the XTR103.



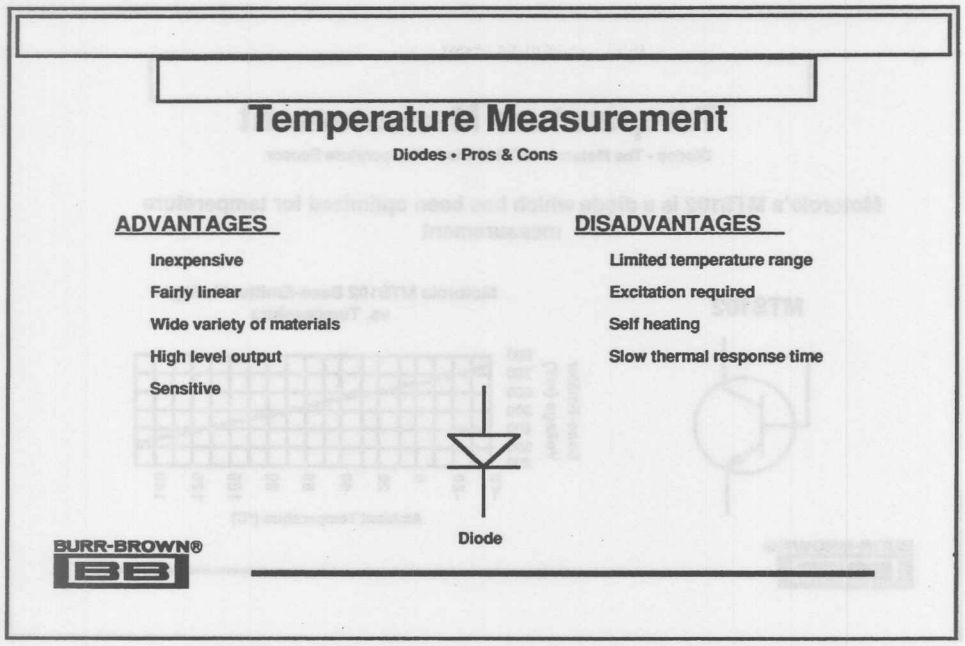
Temperature Measurement

Thermistors • Pros & Cons

The thermistor is very similar to the RTD, with one exception - it is constructed with semiconducting devices instead of metals. "The semiconducting materials, which include oxides of copper, cobalt, manganese, nickel, and titanium, exhibit very large changes in resistance with temperature. As a result, thermistors can be fabricated in the form of extremely small beads" [3]. However, thermistors offer a few advantages over RTDs. Their small size allows them to detect temperatures at pinpoint locations, and their higher initial resistance (usually 3kΩ to 5kΩ) helps to negate the lead resistance errors seen with RTDs. Also, being made of semiconducting materials as opposed to metals, they are usually less expensive than their RTD cousins. As with an RTD, the most likely source for excitation is the current source. There are some vendors, such as Omega, which suggest that a thermistor placed in a Wheatstone bridge which is excited with a voltage will provide precise sensing.

As to not bore you with the similarities of thermistors to RTDs, we will not discuss thermistors in any further detail.

3) James W. Dally, William F. Riley, Kenneth G. McConnell: Instrumentation For Engineering Measurements, p407, John Wiley & Sons, Inc, New York, ©1984

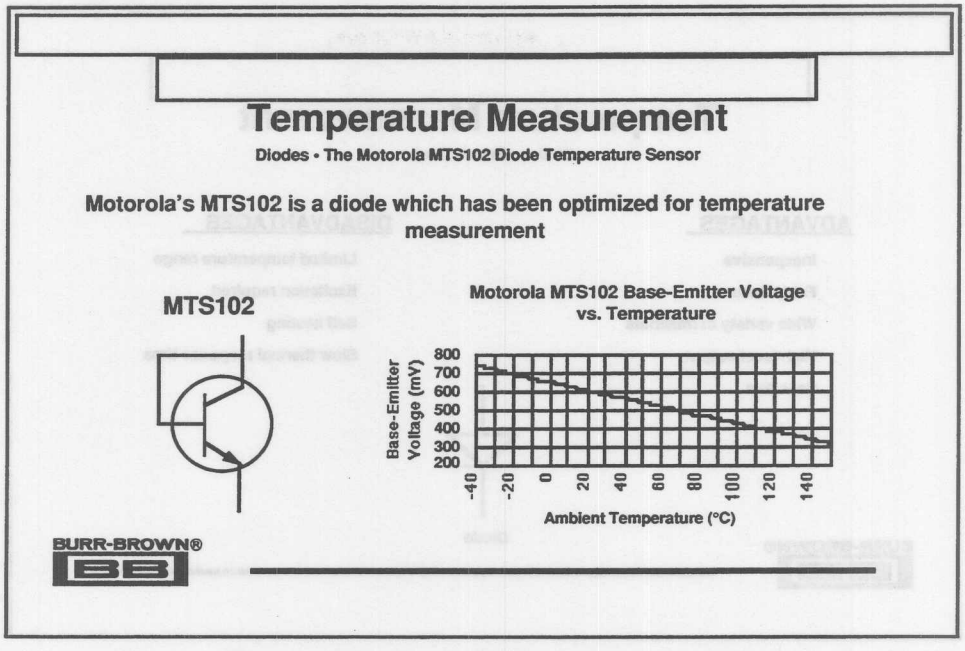


Temperature Measurement

Diodes • Pros & Cons

If a common diode is connected across an ohmmeter, the diode resistance can be measured. If the diode is heated or cooled, a corresponding change in the resistance can be measured (the resistance is inversely proportional to temperature). Since it is apparently the resistance which is changing, a current source is the best alternative for excitation to achieve a linear output.

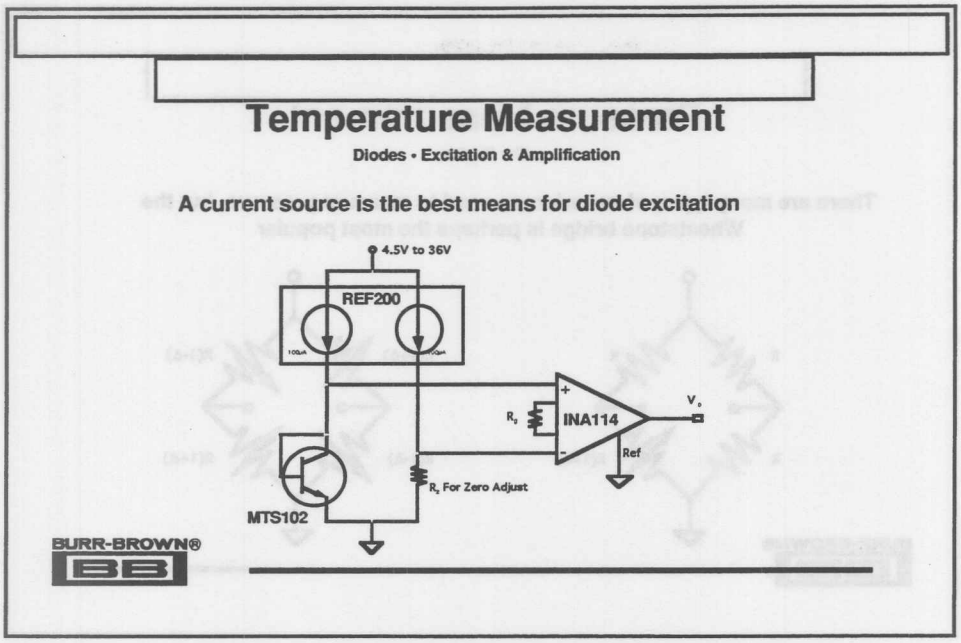
Diodes provide several advantages over some of the other temperature sensing transducers. Primarily, these advantages include cost, linearity, and a high level output (-2mV/°C @ 25°C vs. 50.2µV/°C for a Type "J" thermocouple). However, diode temperature sensors are useful over a limited temperature range (about 200°C max), have a slow thermal response time, and are subject to self heating due to the power dissipated in the diode. Diodes are frequently used as temperature sensors in moderate precision temperature measurement systems.



Temperature Measurement

Diodes • The Motorola MTS102 Diode Temperature Sensor

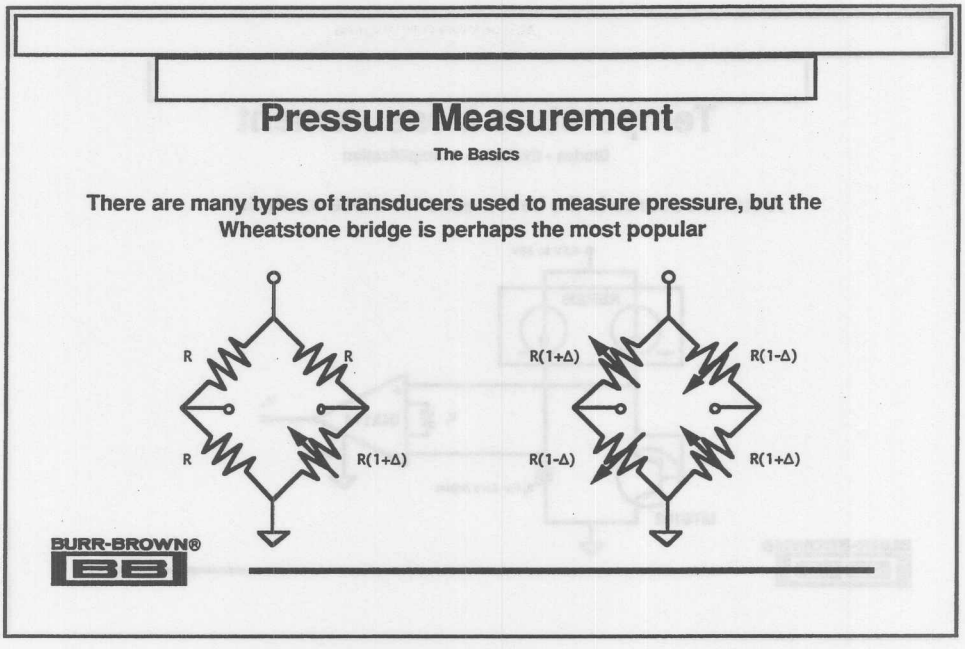
Just about any silicon diode can be used as a temperature measurement transducer. However, the Motorola MTS102 Silicon Temperature Sensor is a diode specifically designed and optimized for this function, and is the topic of our diode-based temperature measurement discussion. The MTS102 is intended for temperature sensing applications in automotive, consumer, and industrial products where low cost is important. Packaged in a TO-92 package, it features precise temperature accuracy of±2°C from -40°C to 150°C, a linear output vs. temperature, and a fast thermal time constant.



Temperature Measurement

Diodes • Excitation & Amplification

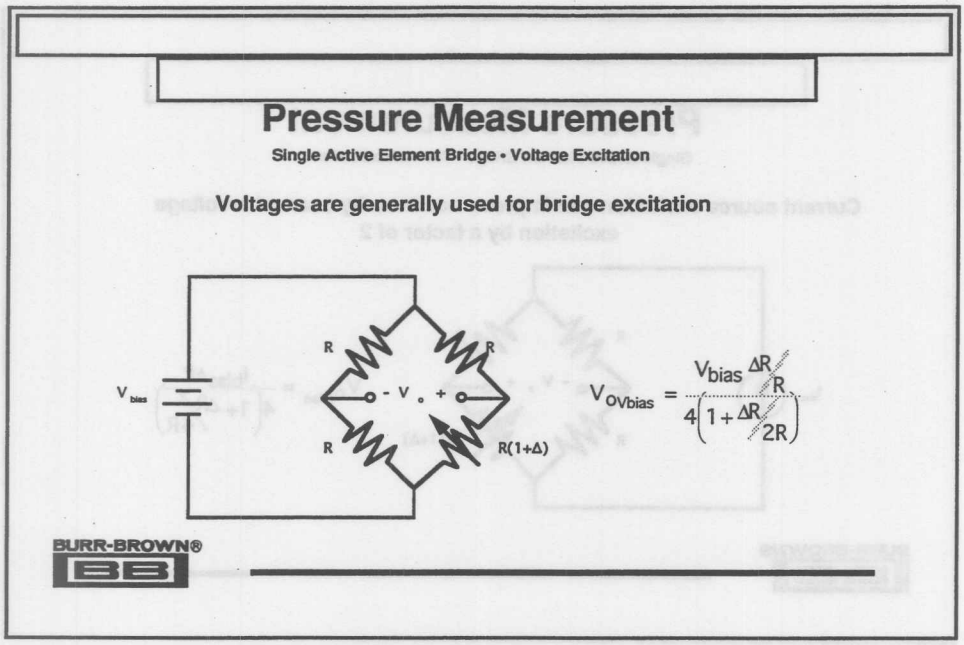
A current source is the best means for diode excitation. In some instances, resistor biasing (2 element bridge with voltage excitation) can provide an adequate approximation, but power supply variations and ripple can cause significant errors with this approach. These problems are exacerbated in applications with low power supply voltages such as 5V single supply systems. Since the MTS102 is specified for 100µA operation, the Burr-Brown REF200 Dual 100µA Current Source/Sink makes the perfect match. One of the REF200's current source can be used for excitation and the other current source can be used in conjunction with R_z for offsetting the output of the amplifier. The INA114 then takes the difference of these two signals to give an output corresponding to the MTS102's temperature. The MTS102 could also be used with the XTR101 or XTR103 current loop transmitters.



Pressure Measurement

The Basics

There are many different types of transducers for sensing temperature, but the same is not true of sensing pressure. Strain gauges are used almost exclusively for this purpose. They are typically piezoresistive elements connected in a Wheatstone bridge. The transducer might also be a single active element of a Wheatstone bridge. There are also strain gauges which have, instead of one, two or four active elements. Due to the similarities of two active element and four active element bridges, four element bridges will be discussed for multiple active element bridges.



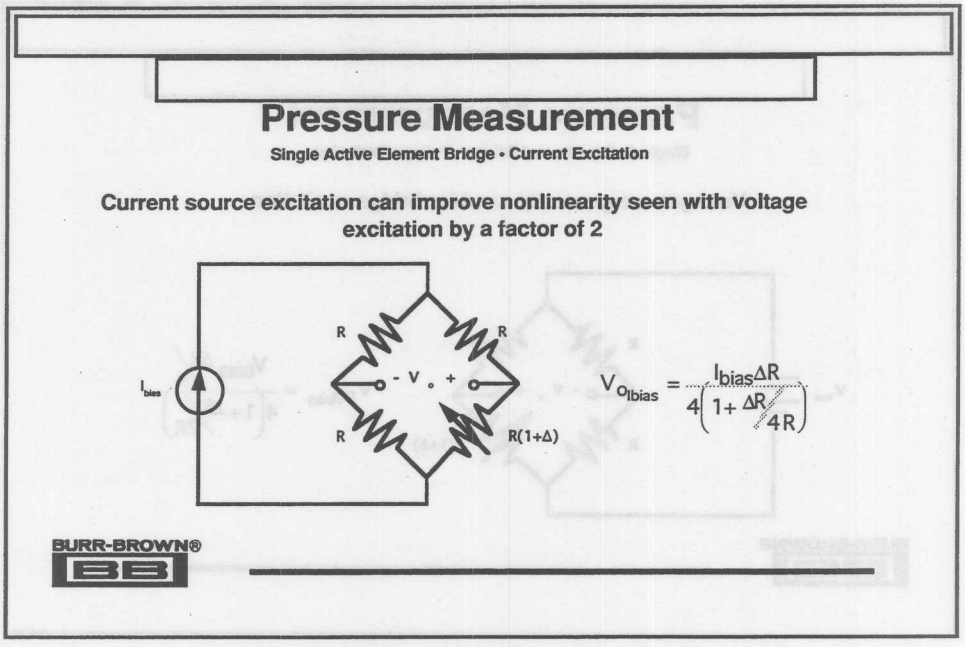
Pressure Measurement

Single Active Element Bridge • Voltage Excitation

A "standard" has developed whereas Wheatstone bridges are usually biased or excited with a fixed reference voltage, and strain gauges are typically specified with a voltage excitation. This voltage will also keep the (-) output of the bridge at $V_{bias}/2$. The overall transfer function for a single active element bridge biased with a voltage is:

$$V_{oVbias} = \frac{V_{bias}\left(\Delta R/R\right)}{4\left(1+\Delta R/2R\right)}$$

However, since ΔR appears in both the numerator and denominator, a nonlinearity is introduced (if a single element changes in a linear fashion, the bridge output does not).



Pressure Measurement

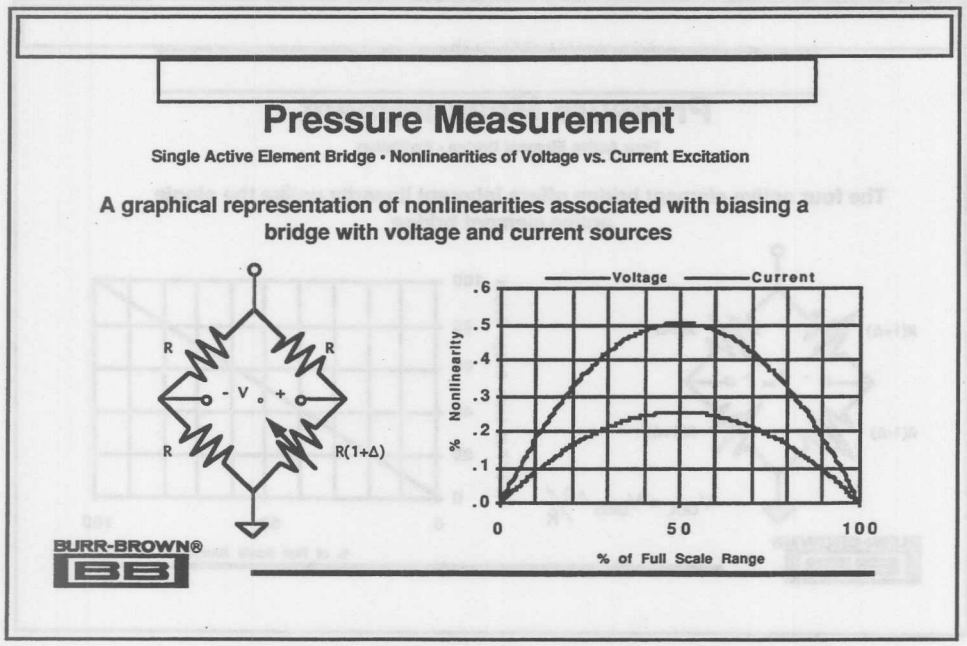
Single Active Element Bridge • Current Excitation

By using a fixed current reference to bias the bridge, the initial nonlinearity can be improved. When a current reference is used, the transfer function of the bridge is:

$$V_{O_{Ibias}} = \frac{I_{bias}\left(\Delta R/R\right)}{4\left(1+\Delta R/4R\right)}$$

Now the ΔR term in the denominator is divided by 4R instead of 2R as with the voltage bias. The result: a 2:1 reduction in nonlinearity error.

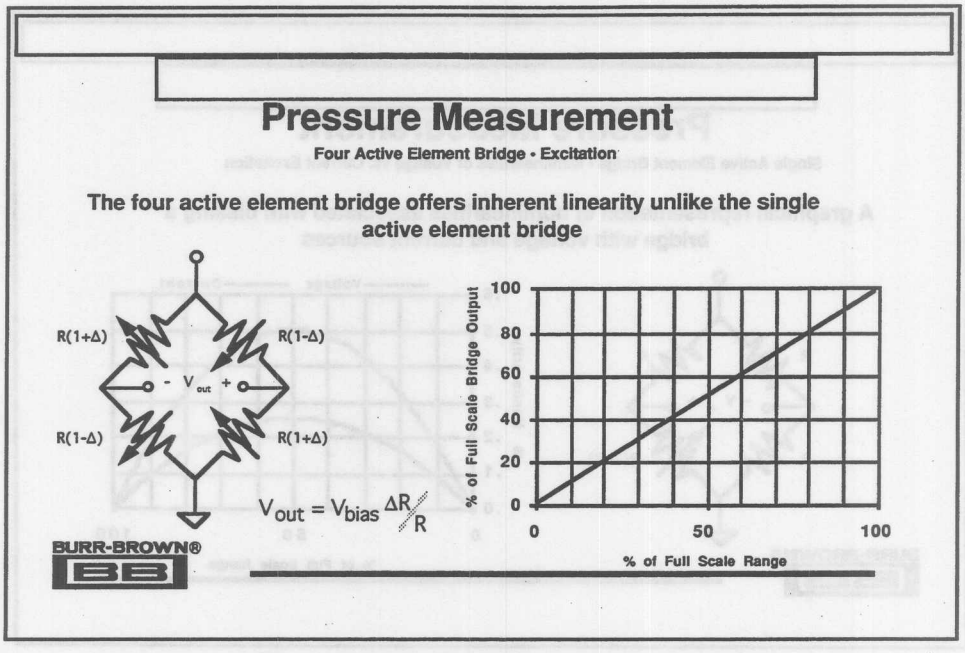
Use current excitation with bridges with caution! Some vendors, such as SenSym use temperature compensation networks in some of their strain gauges, and these temperature compensation networks don't perform very well with current excitation. Before using current excitation with a strain gauge specified for voltages, check with the strain gauge vendor to see if current excitation is acceptable. If the vendor suggests not using current reference excitation, it may be that they have a very similar model which is specified for current excitation.



Pressure Measurement

Single Active Element Bridge • Nonlinearities of Voltage vs. Current Excitation

Shown here is a single active element, 5kΩ bridge. When biased with a 5VDC reference, the bridge will develop a 50mV full scale output. Using a 1mA current reference, the bias voltage across the bridge at null will be 5VDC. However, as the strain gauge starts to output a signal, the overall impedance of the bridge will rise, and therefore the bias voltage across the bridge will also increase. As discussed previously, this will decrease the nonlinearity by 50%. A graphical representation of nonlinearity vs. percent of full scale change is shown here, indicating the overall improvement.



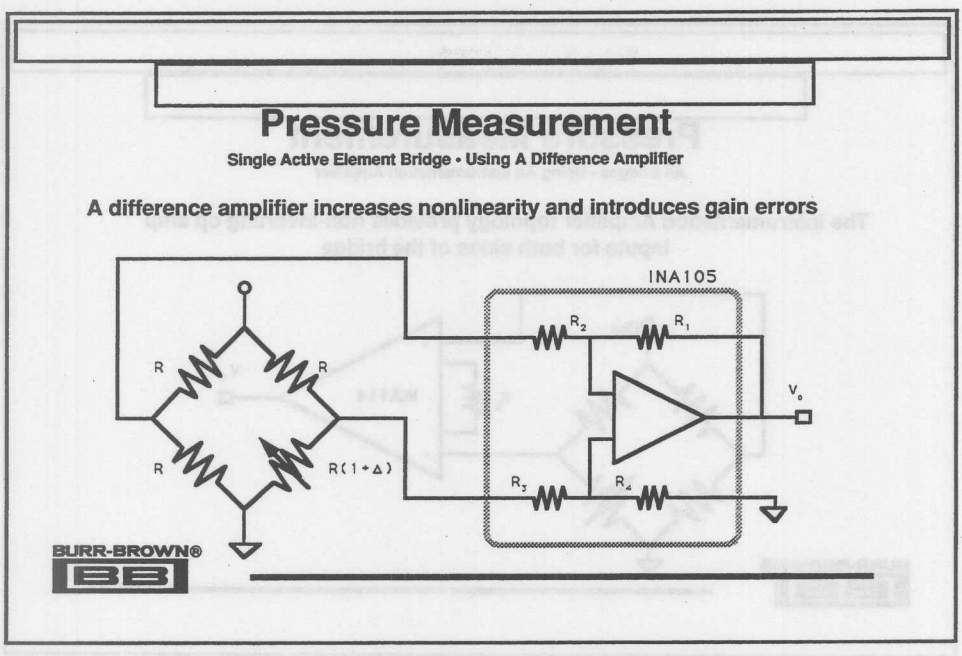
Pressure Measurement

Four Active Element Bridge • Excitation

When a bridge is used which has four active elements, the bridge output is much more simplified. The transfer function for the four active element bridge output is reduced to:

$V_o = \Delta R/R$

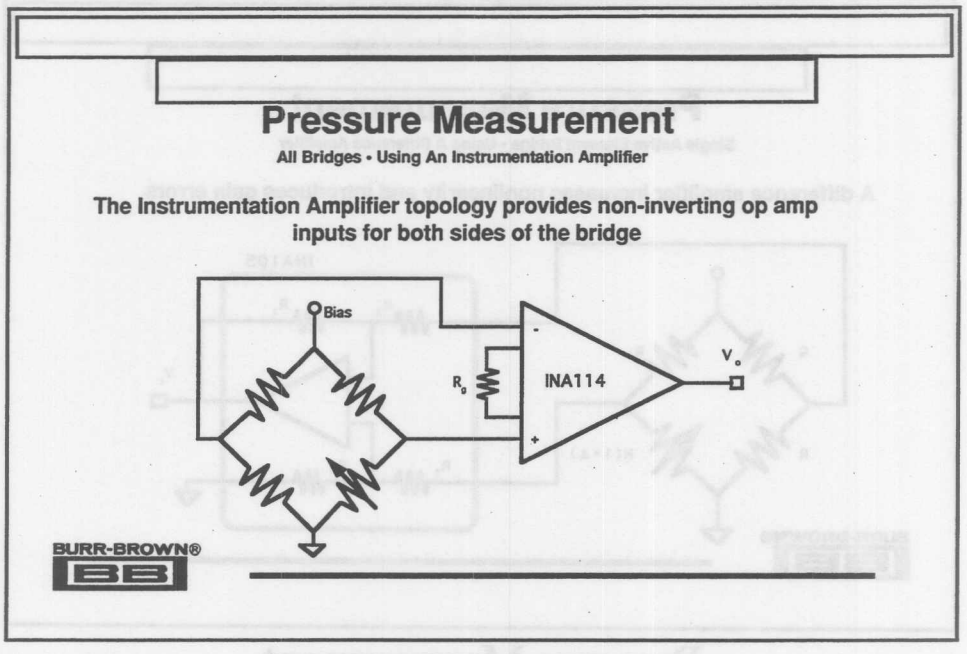
With the ΔR term only in the numerator, the bridge output now exhibits a linear response. This is a very popular form of the Wheatstone bridge due to this linear output. Using current excitation with a four active element bridge will offer no advantages here, as the bridge impedance is always a constant.



Pressure Measurement

Single Active Element Bridge • Using A Difference Amplifier

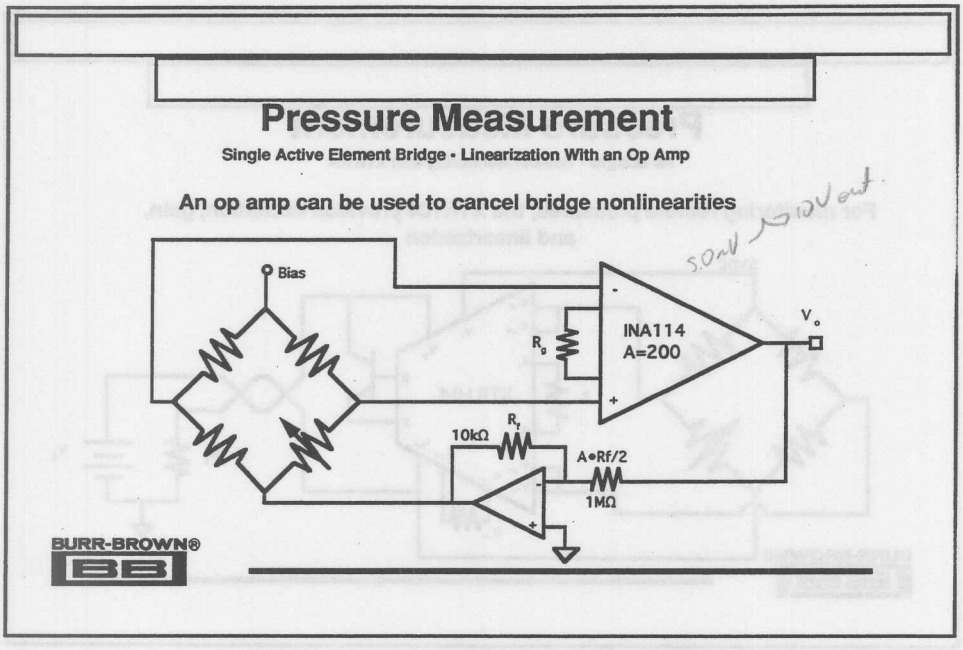
When looking at this circuit initially, you may think that the results would be satisfactory. The bridge outputs a differential signal, and a difference amplifier is supposed to output a signal proportional to the input difference signal while rejecting the common mode voltage. The problem is that the input resistance of the diff amp (summing junction side) is signal dependent. As the bridge leaves null, so does the op amps's summing junction (remember, an op amp's job in life is to keep its summing junction at the same potential as its non-inverting input). This causes a change in currents in the reference side of the bridge. For example, if this had been a 5kΩ bridge with a 50mV full scale output when biased with 5V, the bridge nonlinearity would have been approximately 0.51% (see Slide #4 "Pressure Measurement • Single Active Element Bridge • Nonlinearities of Voltage vs. Current Excitation"). By adding a Burr-Brown INA105 difference amplifier with $R_1=R_2=R_3=R_4=25k\Omega$, the nonlinearity would be increased by approximately 5%, but there would also be a gain error of approximately 13% introduced to the system.



Pressure Measurement

All Bridges • Using An Instrumentation Amplifier

By using an instrumentation amplifier to monitor the bridge, the bridge loading is negligible ($\approx 10^{10}\Omega$) and constant, unlike the pure difference amplifier. For most applications, a bipolar input stage (such as the INA114) is sufficient. But for multi-channel, multiplexed applications, you may find need for a FET input stage instrumentation amplifier (such as the INA111) for best input offset current times multiplexer R_{on} performance. With the FET part, this I•R drop should also be negligible. Single channel mismatch in differential channel resistances of a mux will cause offset errors, while channel to channel mismatches cause channel dependent errors - these are tough to minimize.



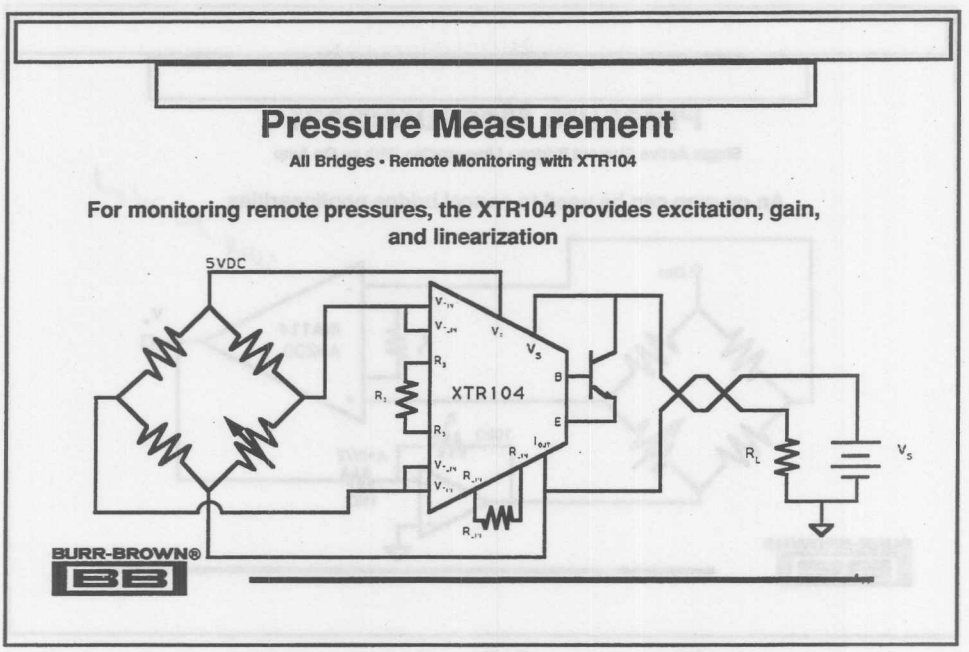
Pressure Measurement

Single Active Element Bridge • Linearization With an Op Amp

Although the four active element bridge offers the advantage of linearity, you may find that it also costs more. If this is the case, and the four active element bridge is outside of your budget, an op amp can be used to correct for the nonlinearities of a single active element bridge.

$$V_o = \frac{A \bullet V_{bias} \Delta R}{4R}$$

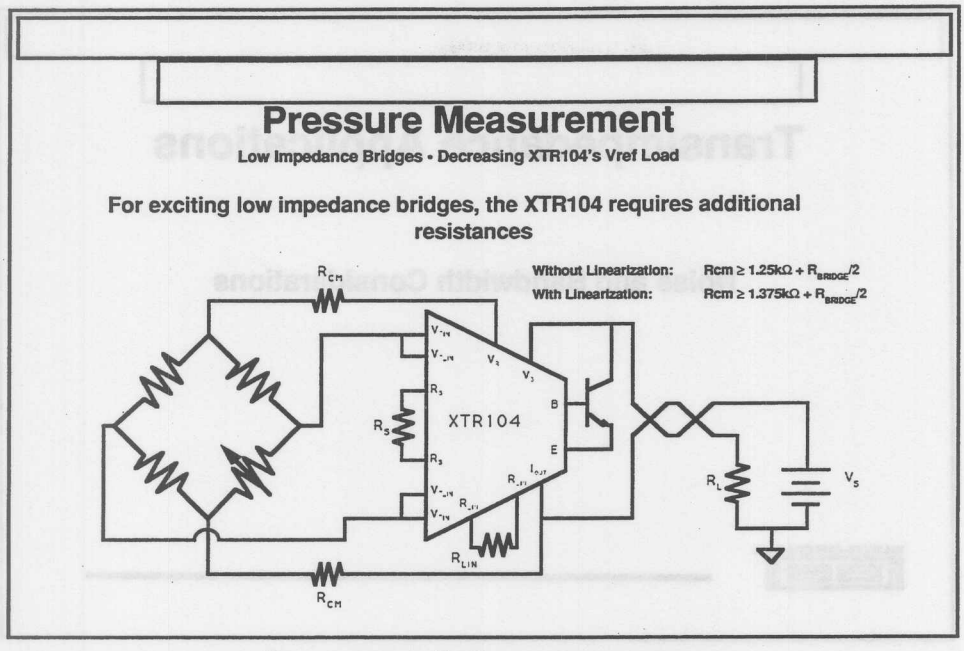
By feeding back a signal that is proportional to the bridge output, nonlinearity is completely removed.



Pressure Measurement

All Bridges • Remote Monitoring with XTR104

Unfortunately, we usually are not monitoring pressures right at our data acquisition systems, and we wind up sending signals over some type of transmission line. The 4-20mA industrial current loop was developed for this purpose. This 4-20mA signal becomes immune to the noise and I•R drops which plague voltage transmission. The XTR104 was designed to provide a complete solution to excitation, signal gain, and linearization of remotely located bridge transducers. Separate V_{lin} inputs have been provided to compensate for both positive and negative nonlinearities. Its 5V reference is capable of driving loads of 2.5kΩ (2750Ω if linearization is used) and linearization can typically be improved by 20:1.



Pressure Measurement

Low Impedance Bridges • Decreasing XTR104's Vref Load

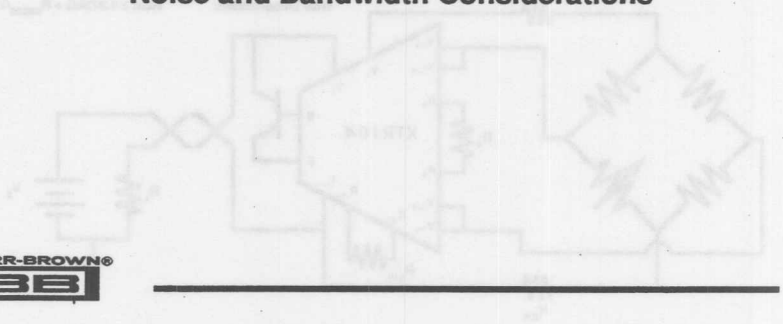
In a circuit with a 300Ω strain gauge impedance, 16.7mA of excitation current would be required at 5V bias. This is 12.7mA greater than the minimum loop current in a 4-20mA current loop. Therefore, when using low impedance bridges with 4-20mA current loops, the overall impedance of the source network must be increased. This does decrease sensitivity, but is absolutely required. For a four active element bridge using these additional resistors, the bridge output is:

$$\text{Vbridge} = \left(\frac{V_{bias} R_{bridge}}{R_{bridge} + 2R_{cm}}\right) \bullet \left(\frac{\Delta R}{R}\right)$$

Since the impedance of the bridge remains fixed with the four active element bridge, no nonlinearities are introduced. However, with the single active element bridge, a 300Ω bridge using 1.2kΩ resistors in both R_{cm} locations will show an improvement in nonlinearity of approximately 1.8x. This is because the voltage across the bridge is allowed to increase with impedance - as in the case with current excitation.

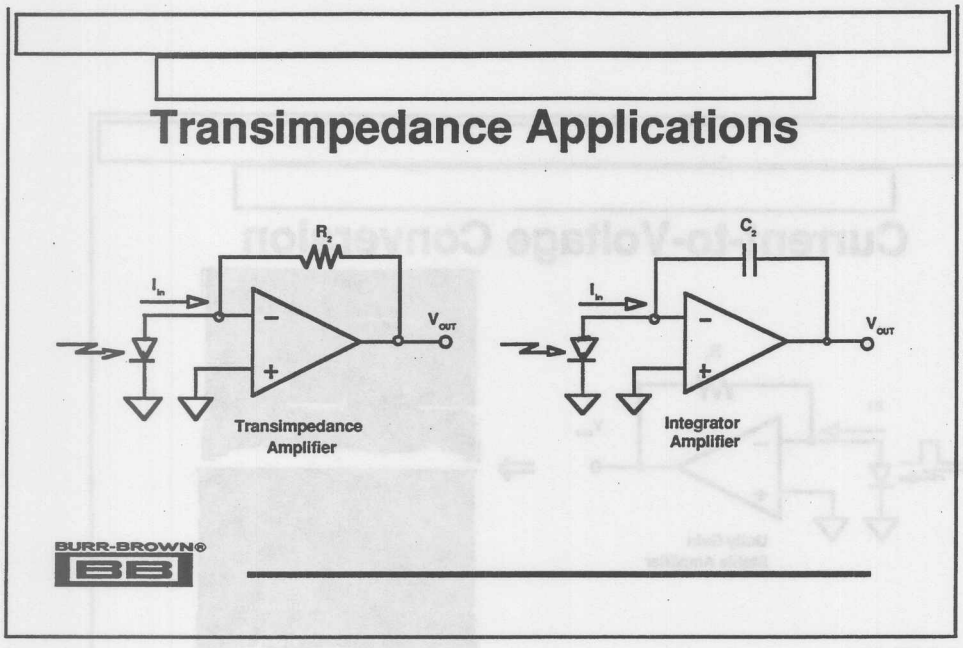
Transimpedance Applications

Noise and Bandwidth Considerations



BURR-BROWN®

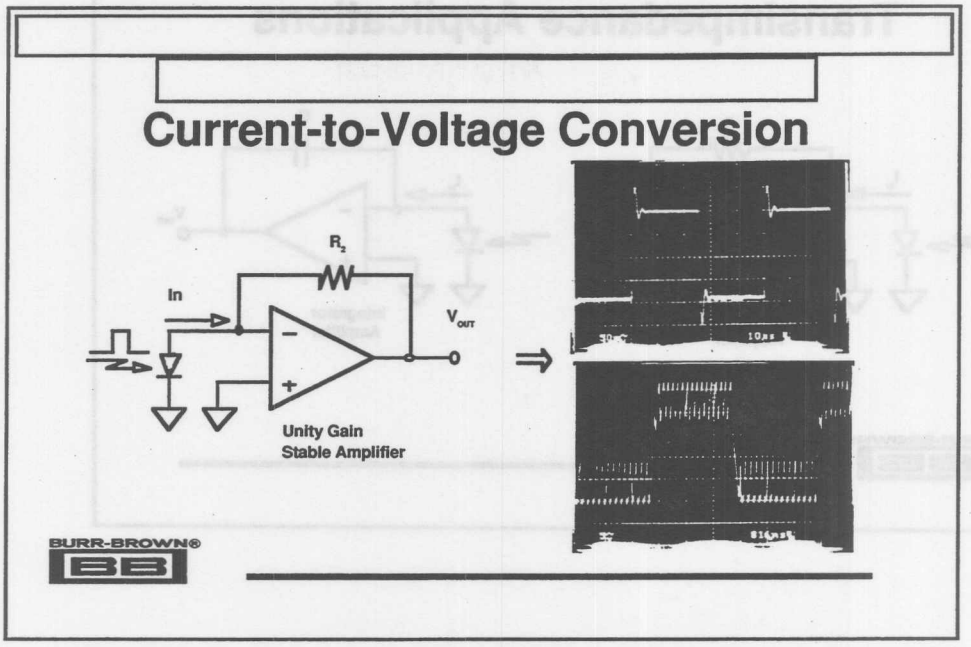
Transimpedance Applications



Transimpedance Applications

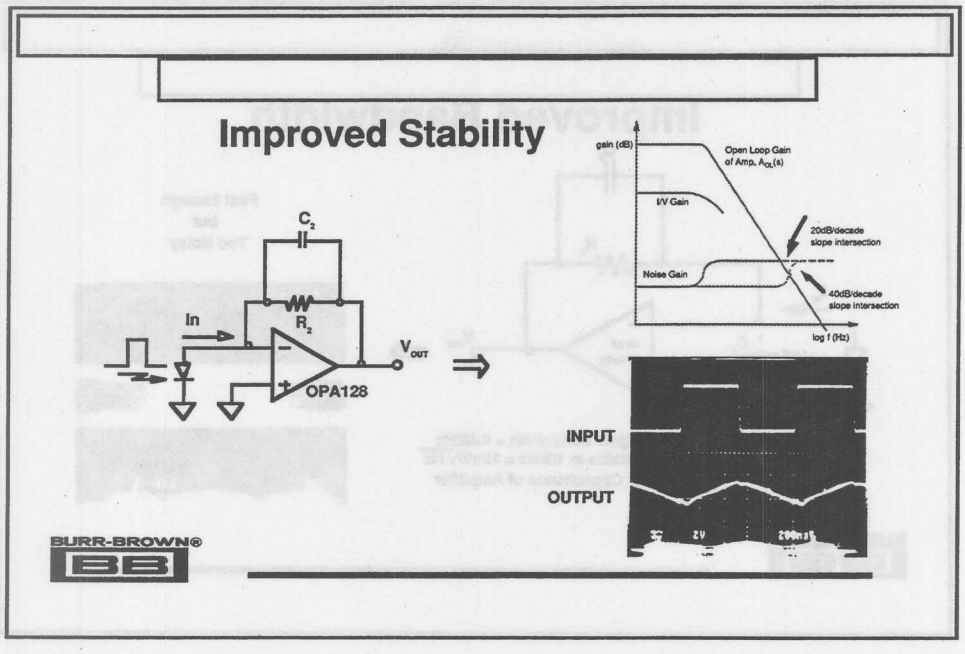
In this portion of the seminar we will engage in a detailed analysis of precision photodiode preamplifier circuits. Two basic design approaches will be analyzed and compared. The first design approach that we will discuss is often called a transimpedance amplifier. The transimpedance amplifier converts the current of the photodiode to a voltage by use of a resistor in the feedback loop of an amplifier. The integrator amplifier converts the current of the photodiode to a voltage by use of a capacitor in the feedback loop of the amplifier. Design trade-offs for both of these circuits will be analyzed and then their noise and bandwidth performance compared.

We will first start with the analysis of the transimpedance amplifier.



Current-to-Voltage Conversion

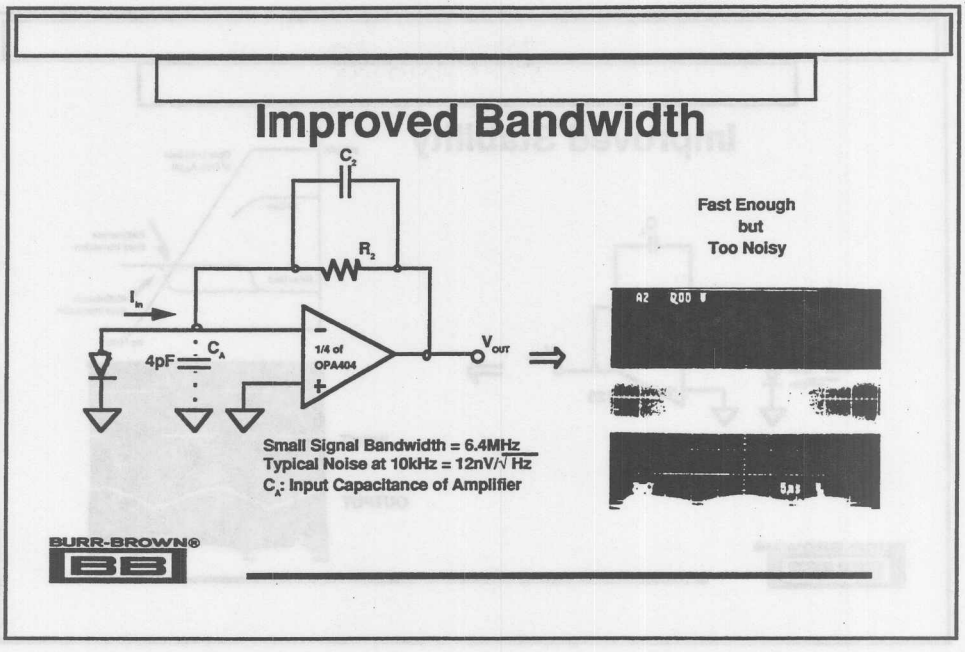
The most obvious way to design a precision current-to-voltage converter is to put a photodiode across the inputs of an FET input amplifier and a resistor in the feedback loop. An FET input amplifier is needed for its low input bias current characteristics. The incident light on the photodiode causes current to flow through the diode. That current also flows through the feedback resistor causing a voltage drop across the resistor. Since the inverting input of the amplifier is kept at a virtual ground with this configuration, the output will change in voltage in accordance with the IR drop across the resistor. A simple solution, often destined for failure. The amplifier step response could have horrible ringing or, worse yet, the amplifier could oscillate.



Improved Stability

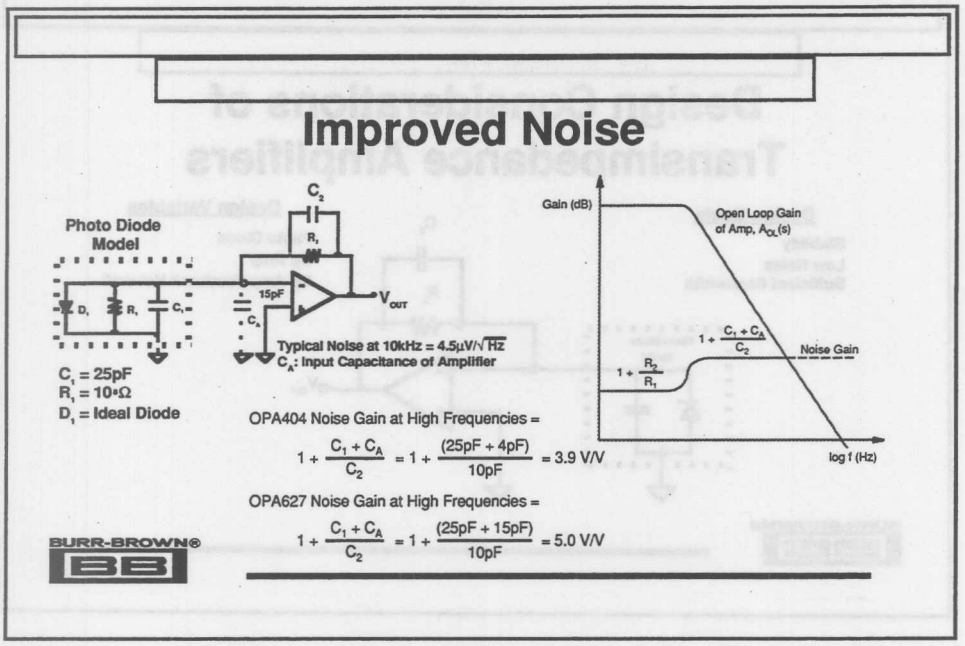
Why did the previous design fail to perform properly? Quite simply, the open loop curve of the amplifier and the noise gain curve of the feedback network have a greater than 20dB per decade difference their in slopes at the intersection. If that doesn't seem simple to understand, don't worry, we'll cover the material later. But for now, the ringing problem of the previous design can be solved by adding a capacitor in parallel with the resistor in the feedback loop of the amplifier. In the bode plot on the slide, the lower noise gain curve represents the transimpedance amplifier without C_2 in the feedback loop. The upper noise gain curve represents the transimpedance amplifier with C_2 in the feedback loop.

The ringing problem is solved and we start to characterize the performance of the circuit. All looks good except for the signal bandwidth. The added capacitor reduced the signal bandwidth. A faster amplifier should solve this problem.



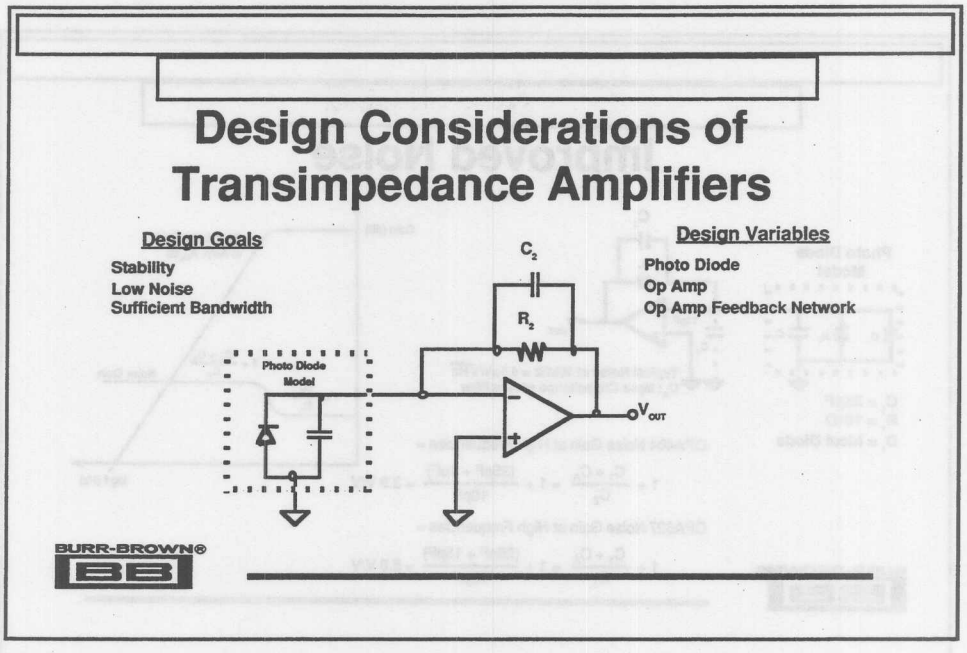
Improved Bandwidth

The OPA404 is selected over the OPA128 because of its bandwidth. Now the capacitor, C_2 can be reduced, which will increase the signal bandwidth of the circuit. The bandwidth performance looks great! Looking further, we consider the signal-to-noise performance of the circuit. The noise of this circuit may or may not be a problem, but for this discussion, let's assume that it is too noisy. The quad amplifier, OPA404, originally was selected for its bandwidth performance and not noise performance. In many transimpedance applications the OPA404 is sufficient. In addition to its low bias current, it is also a board saver because it is a quad. But for this example, the output of the circuit is too noisy. The obvious solution is to select a lower noise FET input amplifier or a cascoded filter. Let's consider a lower noise amplifier.



Improved Noise

The OPA627 is a low noise, wide-bandwidth, FET input amplifier. This looks like the perfect solution to this application problem and so we check the noise. Bench testing shows that there is a slightly higher peak-to-peak noise at the output of the amplifier. Analysis of the problem shows that the input capacitance of the amplifier is significantly higher than input capacitance of the OPA404, which was 4pF. If the parasitic capacitance of the photodiode had been larger, the OPA627 substitution would have reduced the noise. A high input capacitance has an impact on the gain of high frequency noise. As shown in the graph, the high frequency noise of the OPA627 is gained by one plus the capacitance on the input of the amplifier divided by the capacitance in the feedback of the amplifier. The capacitance on the input of the amplifier is the parallel combination of the photodiode parasitic capacitance and the input capacitance of the amplifier. If the photodiode parasitic capacitance is low, such as 25pF, the noise gain of the OPA404 at high frequencies will be 3.9 and the OPA627 high frequency noise gain will be 5. As the photodiode capacitance is increased, the OPA627 noise performance becomes a better alternative.

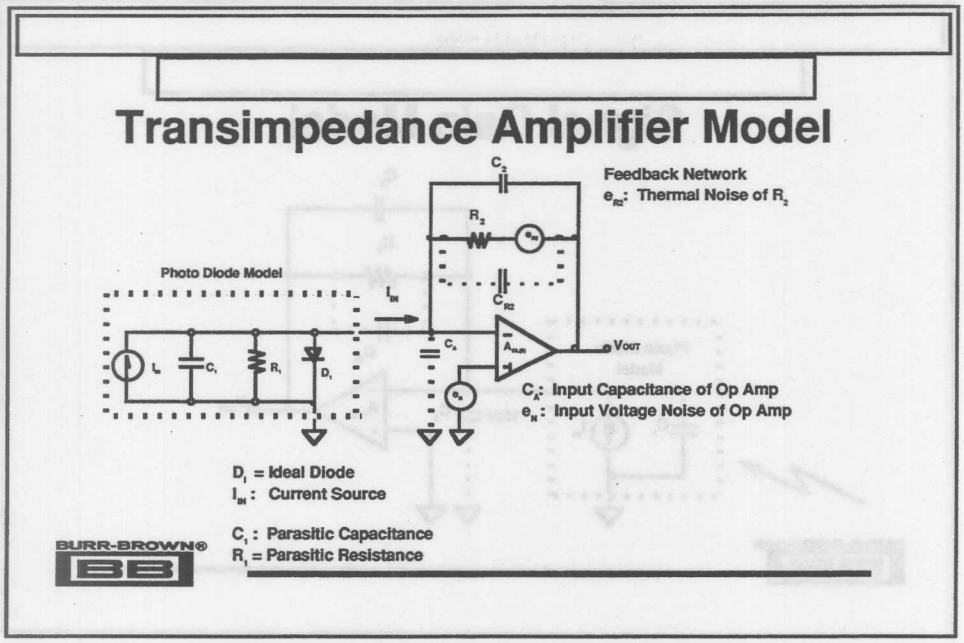


Design Considerations of Transimpedance Amplifiers

The final transimpedance amplifier solution should be sufficiently stable with low enough noise to obtain the desired resolution of the output signal. In addition, the bandwidth should be wide enough to accommodate the speed of the input signal.

The variables in this design problem are the photodiode, the op amp and the op amp's feedback network. If these three variables affected only one performance specification at one time, the optimization of this circuit would be trivial, however, that is not the case.

The photodiode is primarily selected because of it's light response characteristics, however, the parasitic capacitance has a profound impact on the noise gain and the bandwidth of the transimpedance amplifier. The op amp should be a low input bias current amplifier, so not to compromise the resolution of the input signal. Additionally, the noise and bandwidth of the amplifier are critical specifications to consider. Finally, the feedback network affects the signal bandwidth as well as the noise bandwidth of the application. The feedback resistor, R_2, also contributes thermal noise directly to the output of the transimpedance amplifier.

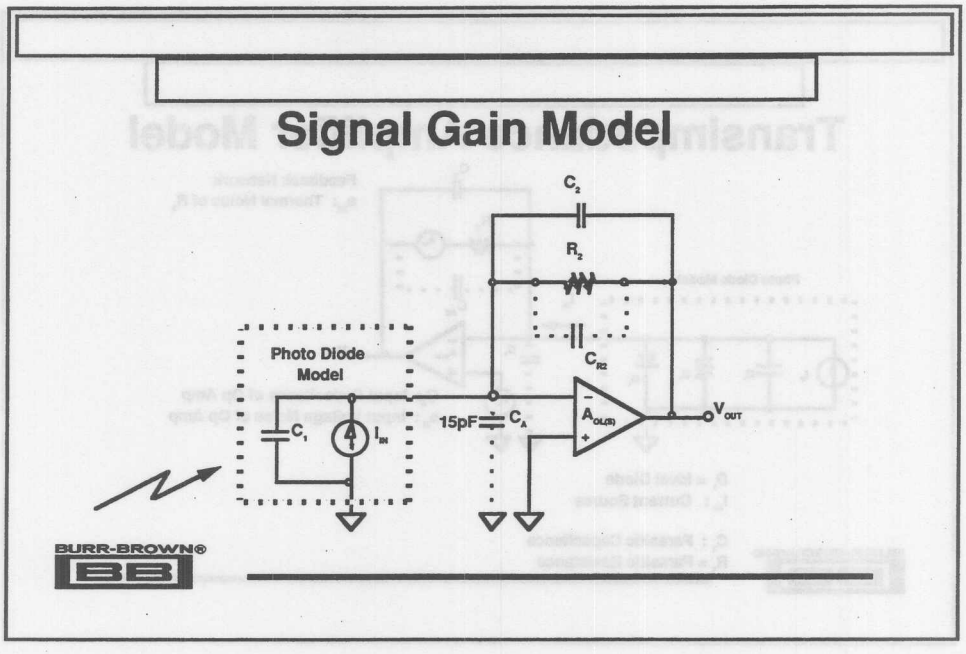


Transimpedance Amplifier Model

This circuit model is used to evaluate the various elements of the performance of the transimpedance amplifier. The photodiode is modelled as an ideal diode in parallel with a current source and parasitic a resistor and capacitor.

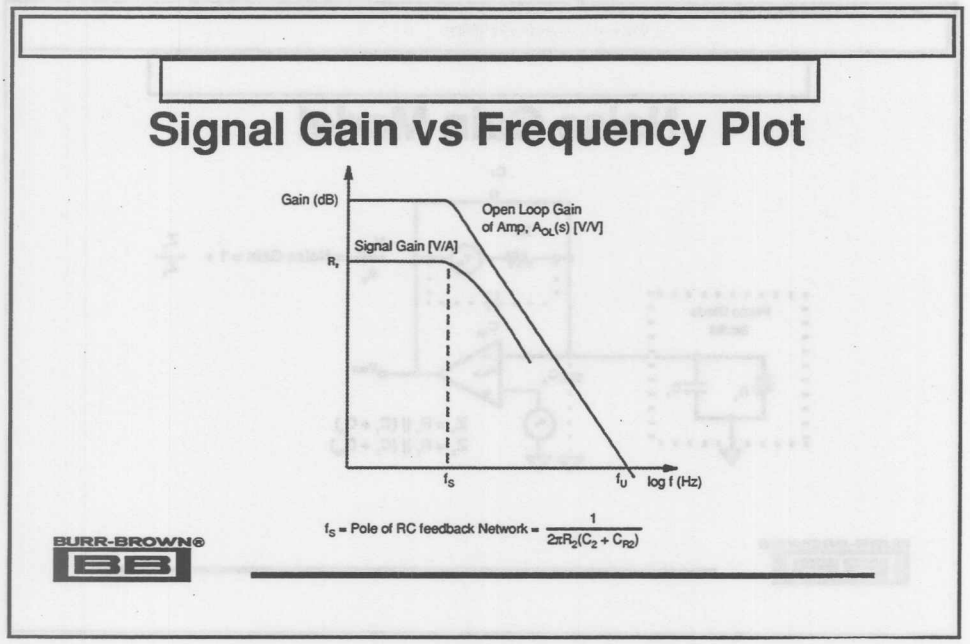
The op amp open loop gain over frequency or more appropriately the bandwidth of the amplifier is modelled in the op amp block. The input capacitance of the op amp, C_A, is equivalent to the differential capacitance plus the common-mode capacitance specified in the op amp data sheet. Additionally, the input voltage noise of the op amp is modelled with the voltage source, e_N. For this discussion, it is assumed that only FET input amplifiers are used, so consequently, the input current noise is negligible.

The feedback network consists of a parallel resistor, R_2, and capacitor, C_2. The ideal resistor is modelled with its thermal voltage noise in series and its parasitic capacitor in parallel. The parasitic capacitor, CR_2, is usually 0.5pF depending on the resistor selected and PC Board layout.



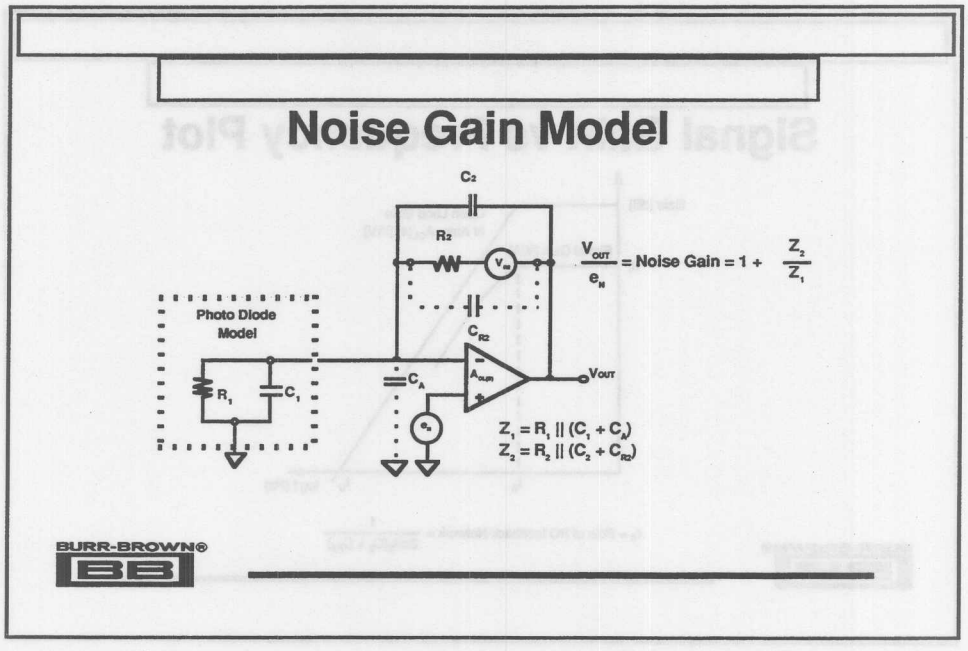
Signal Gain Model

The signal gain of the transimpedance amplifier can be evaluated with this model. The 3dB bandwidth is determined by the pole created by the RC feedback network. A circuit limitation that is often over looked is the parasitic capacitance of the feedback resistor, R_2. Its value is approximately 0.5pF. If for example, the feedback resistor is 10MΩ the pole generated by the resistor and its parasitic capacitance is equal to 32kHz.



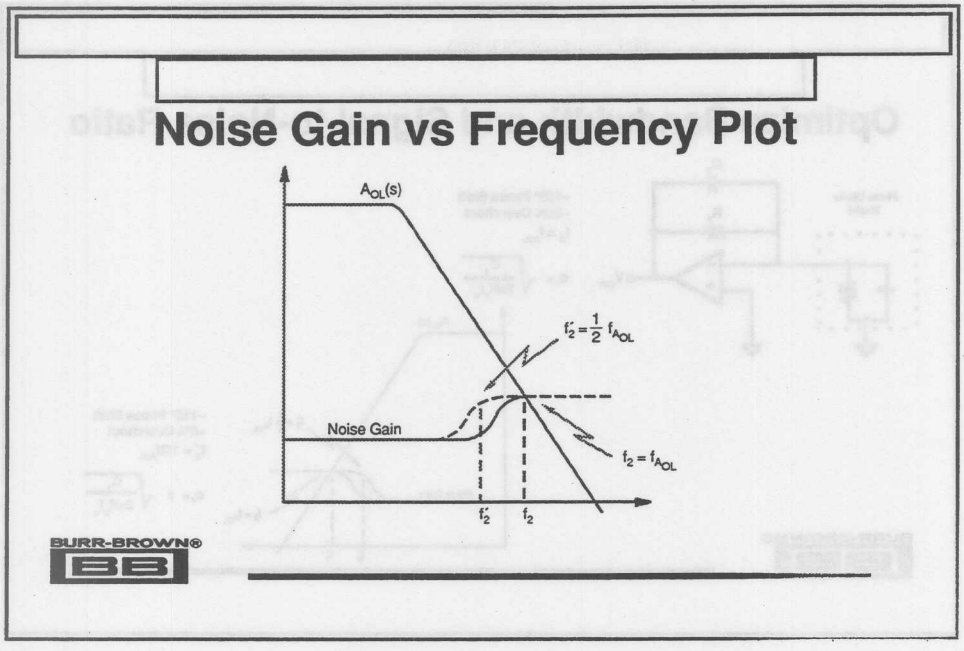
Signal Gain vs Frequency Plot

The DC signal gain of V_{OUT} over I_{IN} is equal to R_2 and the units are volts per amps. The signal pole, f_S, is shown in this bode plot.



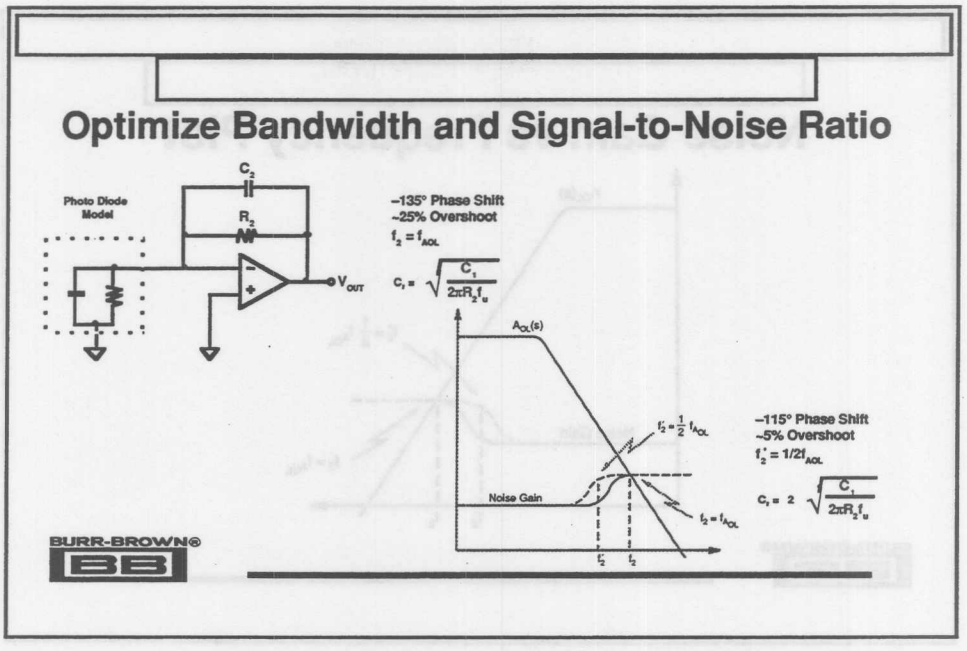
Noise Gain Model

The noise gain of the transimpedance amplifier can be evaluated with this model. The transfer function for this model can be calculated as if the amplifier were in a non-inverting gain, where the amplifier noise is used as the signal source, hence the term noise gain.



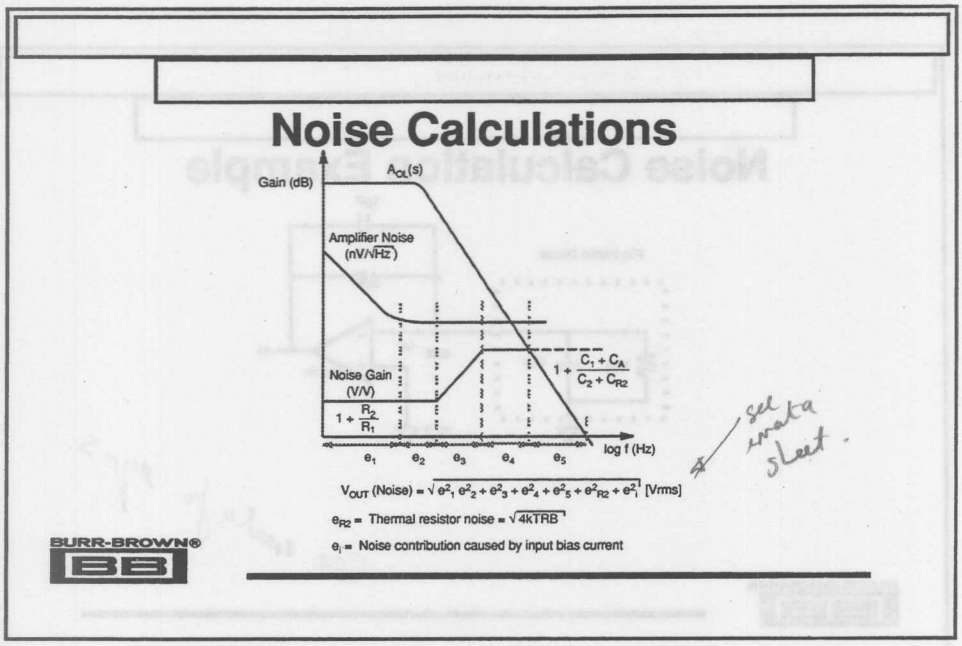
Noise Gain vs Frequency Plot

The DC noise gain of the transimpedance circuit is dependent on the resistors in the circuit. The high frequency noise gain of this circuit is dependent on the capacitors. To optimize the noise and bandwidth performance of the transimpedance amplifier, the pole, f_2, should occur at or slightly before the point where noise gain plot intersects the open loop gain curve of the amplifier. Another words, f_2 should be equal to or less than f_{AOL}. If f_2 is greater than f_{AOL}, the difference in the slopes of the noise gain curve and open loop gain curve can be greater than 20dB/decade which may cause an unstable condition.



Optimize Bandwidth and Signal-to-Noise Ratio

An optimum signal bandwidth and signal-to-noise ratio can be designed into the circuit by placing the pole of the feedback network at the same frequency where the noise gain curve crosses the open loop gain curve of the amplifier. This frequency is the geometric mean of the noise gain and the open loop gain of the amplifier. If the circuit is designed so that f_2 equals f_{AOL}, the phase shift will be -135° with an overshoot of 25%. On the other hand, if a 25% overshoot is too high, f_2 can be designed to be less than f_{AOL} with a small increase in noise.



Noise Calculations

The noise performance of a transimpedance amplifier can be derived by calculations or by simulations. In order to calculate the noise performance of the circuit a piece wise approach can be used with reasonably good results. Although this may seem tedious, the exercise is fairly instructional.

In this slide, the noise evaluation has been separated into seven parts. The first five parts of the equation deal with the transimpedance noise gain versus the voltage noise of the amplifier. In region one, the 1/f noise of the amplifier is gained by the DC gain of the circuit. The amplifier noise is specified in nano volts per root hertz, so the analysis is compete when the average noise over the region is multiplied by the square root of the bandwidth of that region. For FET amplifiers, the 1/f region is usually from DC to 100 or a 1000Hz. The square root, of say 1000Hz is equal to 31.6. Quick calculations prove that the contribution to noise in this low frequency region is relatively low.

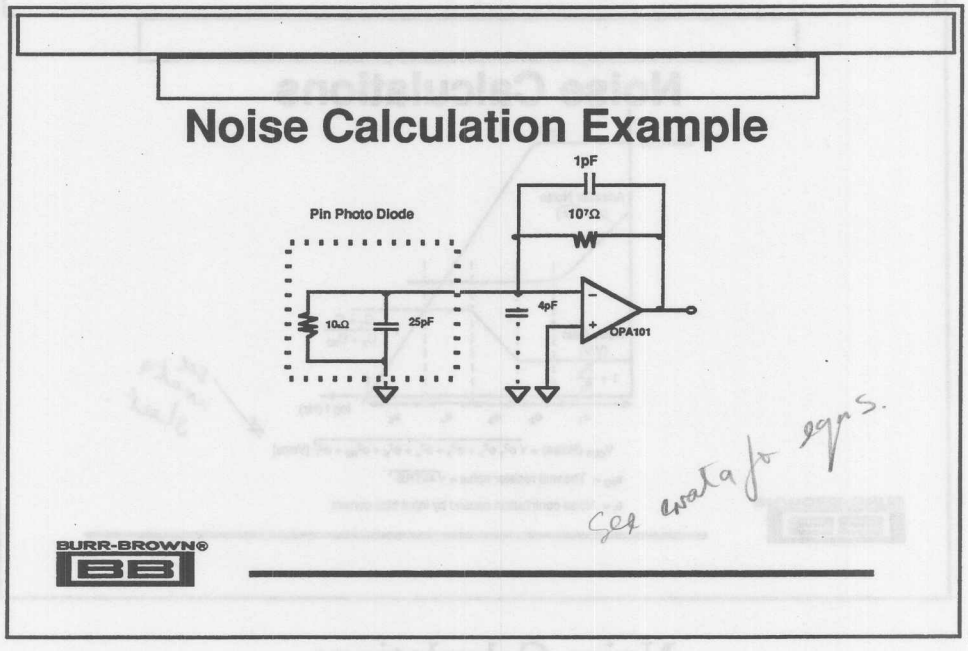
In the second region the broad band noise of the amplifier is multiplied by the DC gain. Again the average noise is multiplied by the square root of the bandwidth of that region, and the contribution to noise of this region is also usually relatively low because of its location in the lower frequency range.

The third, fourth and fifth regions are calculated in the same manner, each region contributing more to the overall noise of the circuit.

The sixth part of the noise equation represents the noise contribution of the feedback resistor, R_2. The noise contribution of this component may or may not be significant depending of the magnitude of R_2.

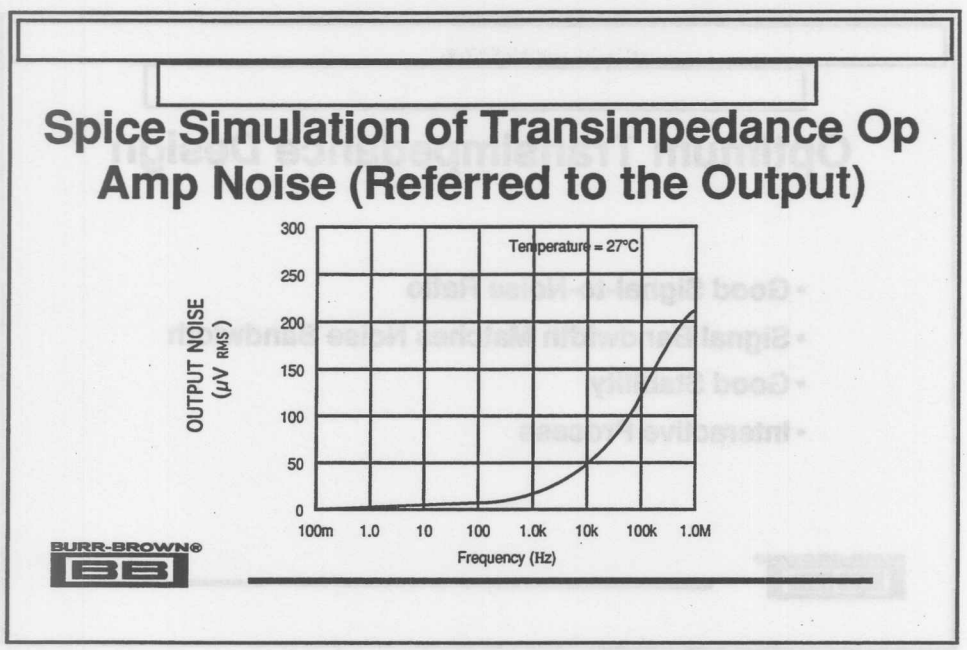
The seventh part of the noise equation represents the noise contribution of the current noise of the amplifier. With FET amplifiers, this noise is proportional to the input bias current. An amplifier with an input bias current in the range of several pico amps will have current noise in the range of a few femto amps per root hertz. As mentioned before, the current noise of the FET amplifiers in a transimpedance amplifier usually don't effect the overall noise performance of the circuit.

These calculations will quickly demonstrate where the highest noise contribution is coming from and make it easier to refine the design.



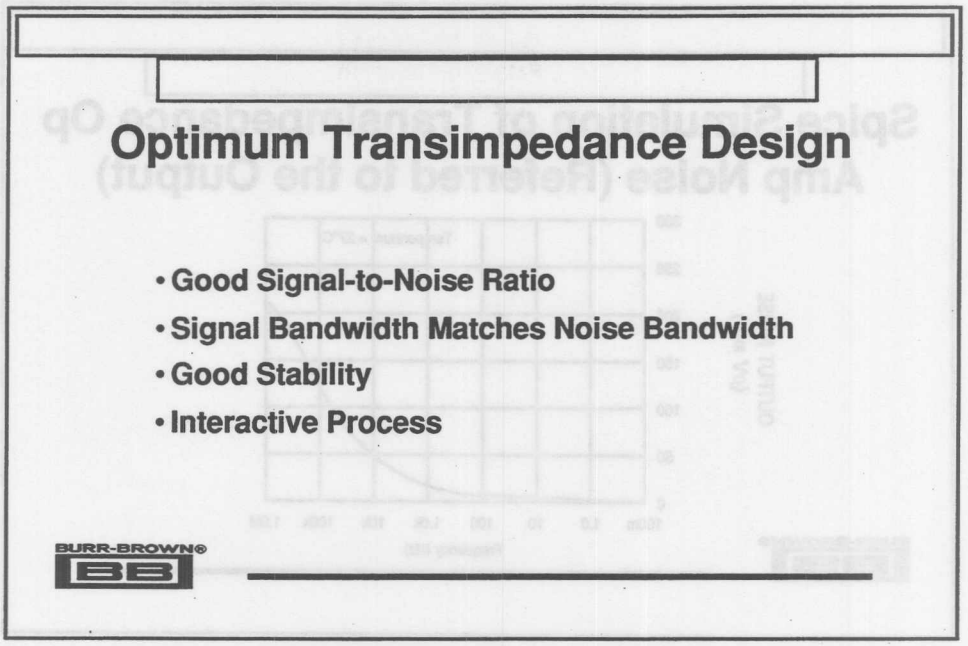
Noise Calculation Example

As an example, an OPA101 op amp and a typical small geometry pin diode with sensitivities in the range of 0.5 amps per watt is shown in this slide. Since the noise calculations are always performed as the square root of the sum of the squares, the noise in regions four and five and the resistor noise dominate the calculated total noise. For this topology, noise could be reduced by the pole caused by the feedback network to a higher frequency, which would reduce the bandwidth of region four.



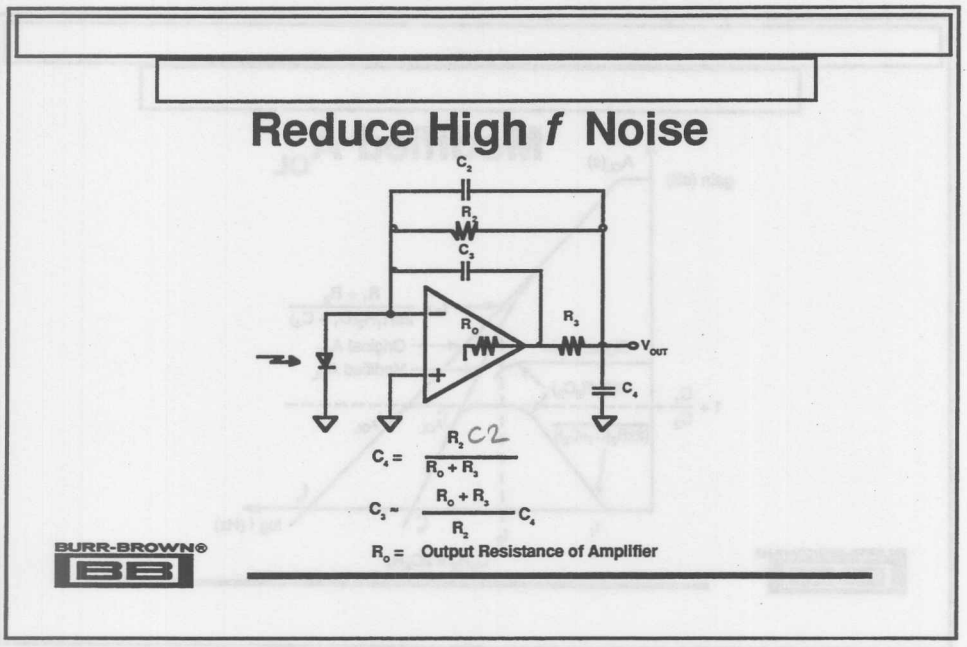
Spice Simulation of Transimpedance Op Amp Noise (Referred to the Output)

The same information is contained in a Spice simulation of the circuit. This plot shows the cumulative noise versus frequency of a transimpedance amplifier. Notice that the rms total noise is very low until 10kHz and more. If the designer of this transimpedance circuit spends their time reducing noise in the lower frequency range, the time will definitely be wasted.



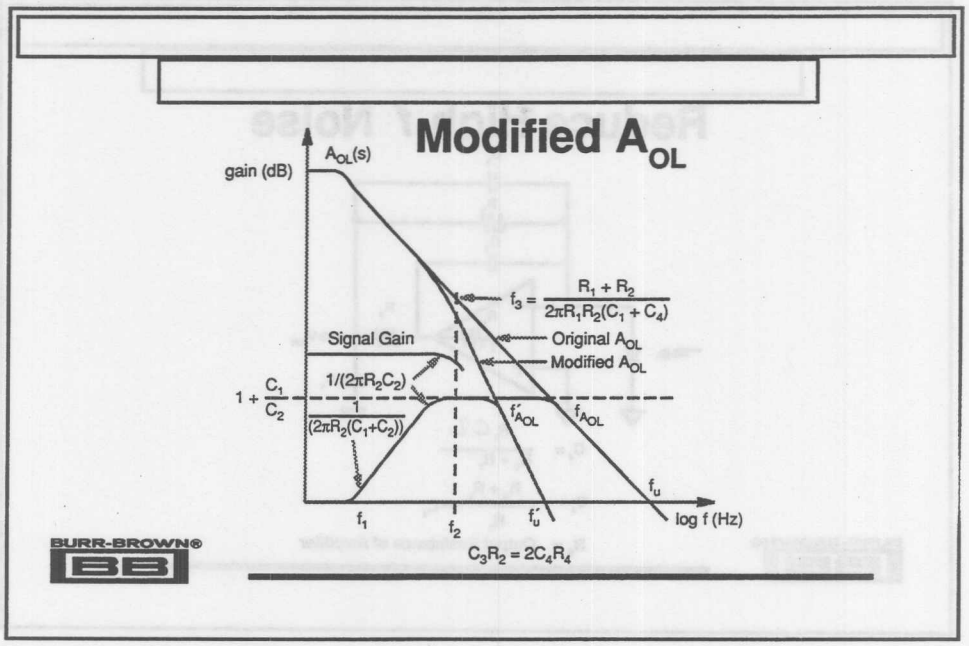
Optimum Transimpedance Design

The transimpedance amplifier design should have a good signal-to- noise ratio. This means that the maximum signal output swing should be equal to the maximum amplifier output swing whenever possible. Secondly, the circuit signal bandwidth should be equal to the noise gain bandwidth. If it is known that the signal bandwidth is fairly low, a low bandwidth amplifier should be chosen in order to reduce high frequency noise. Thirdly, stability is an obvious requirement and easily designed in with the feedback capacitor. And finally, the design of a transimpedance amplifier requires several iterations to get optimal performance from the circuit. The design formulas offer a great deal of insight as to where the problem areas are in the circuit. A more detailed description can be found in the application note section.



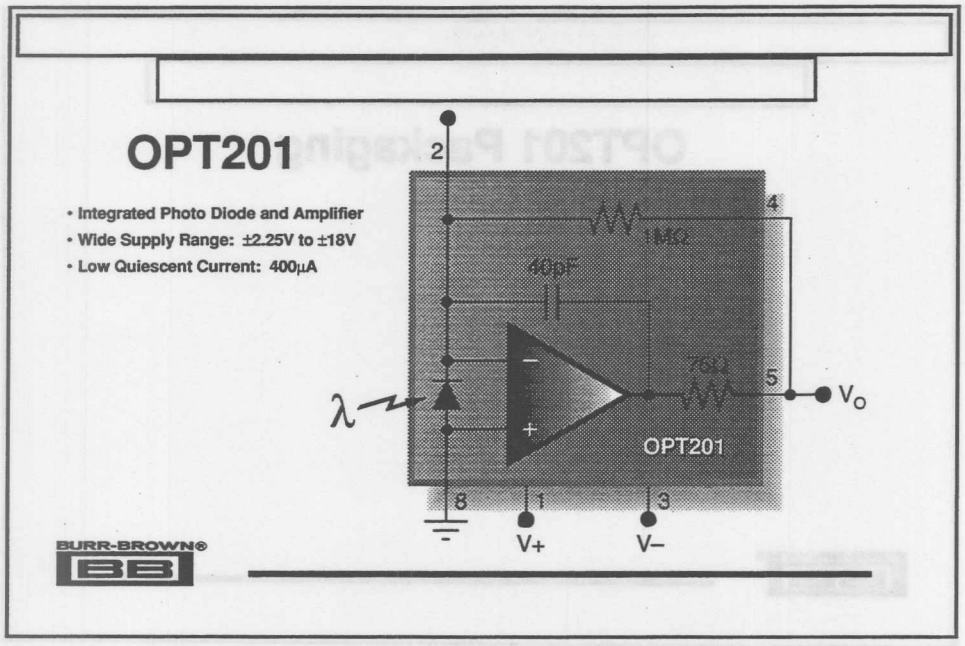
Reduce High f Noise

The transimpedance topology is best suited for high level input currents and wide bandwidth applications. Variations on the classical transimpedance amplifier can improve the performance even further. For example, R_3, C_3 and C_4 can be added to attenuate the noise at the higher frequencies without compromising the signal bandwidth.



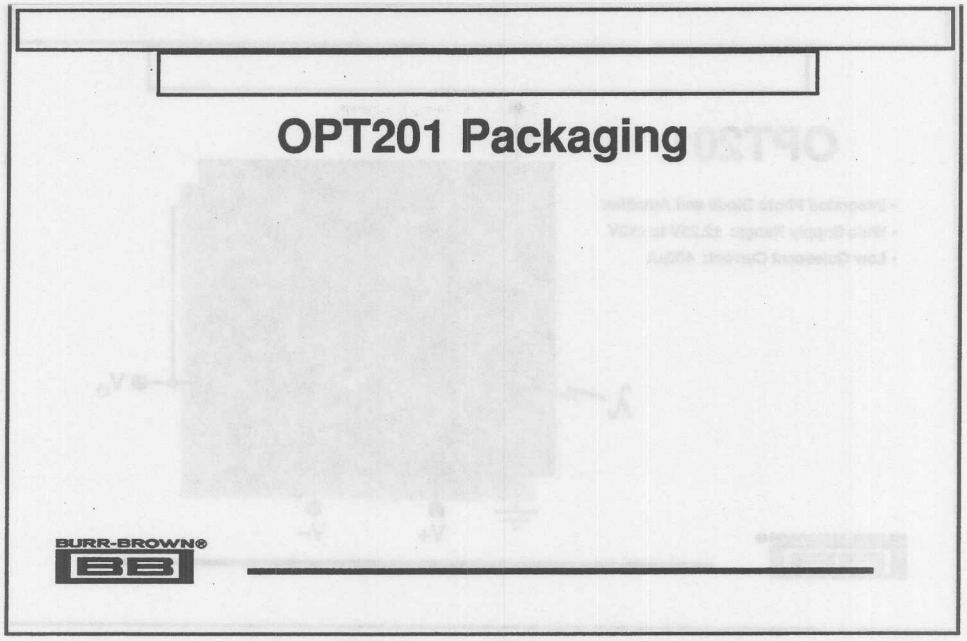
Modified A_{OL}

This circuit adds a second pole, formed by R_3 and C_4. Using the formula at the bottom of this slide, the noise gain transfer function is a 2-pole Butterworth type. This modification reduces the noise by a factor of three.



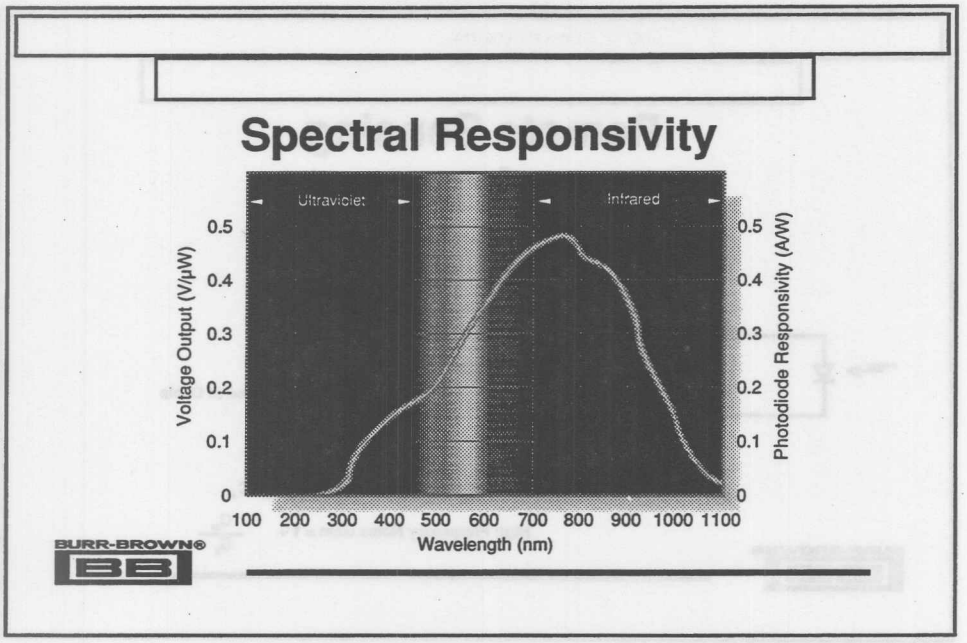
OPT201

This variation on the transimpedance design is used in the OPT201. The OPT201 is an opto-electronic integrated circuit containing the photodiode and transimpedance amplifier in the same package. This integrated combination eliminates the problems commonly encountered in discrete designs such as design optimization problems in production and gain peaking due to stray capacitance. If the internal feedback network is used, the signal bandwidth is 4kHz with typical noise referred to the output of $30\mu V_{rms.}$



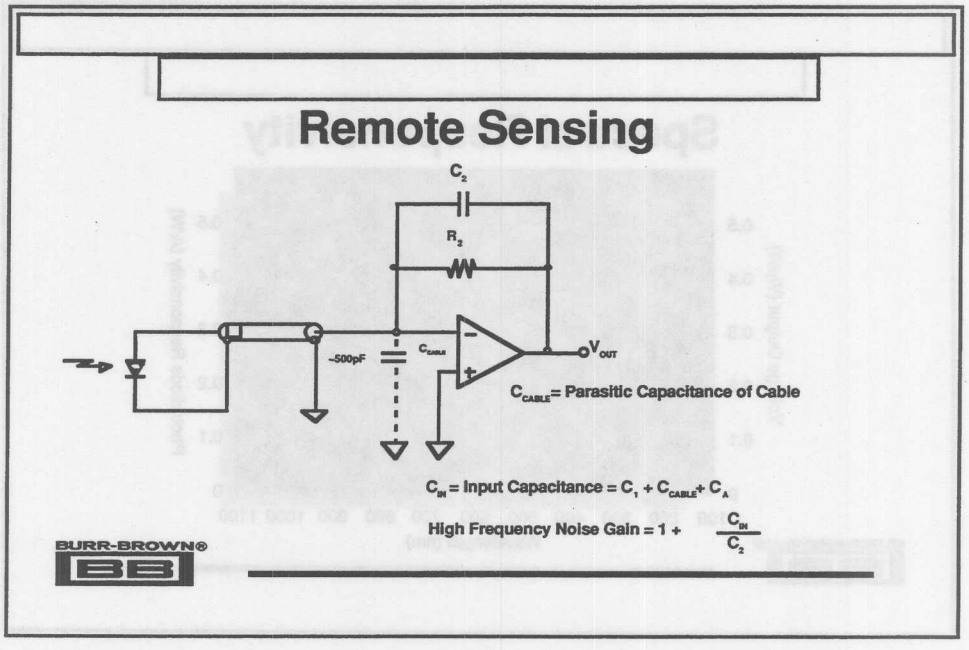
OPT201 Packaging

The OPT 201 uses a unique packaging technology where the photo diode/amplifier monolithic chip is encased in a clear plastic DIP. This packaging technology, specifically developed for the OPT201, allows light to pass directly to the photo sensor, while the amplifier converts the light input signal to a voltage output.



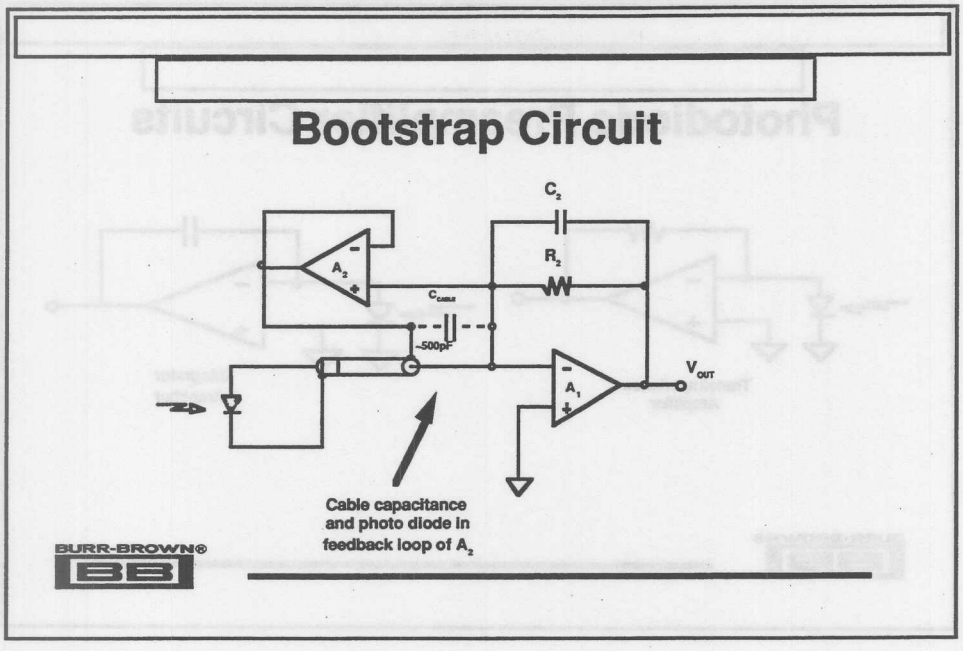
Spectral Responsivity

The spectral responsivity of the photo diode is optimized for infrared light, with its peak at typically a 770µm wavelength. The OPT201 is ideally suited for applications such as medical or laboratory instrumentation, position and proximity sensors, photographic analyzers or smoke detectors.



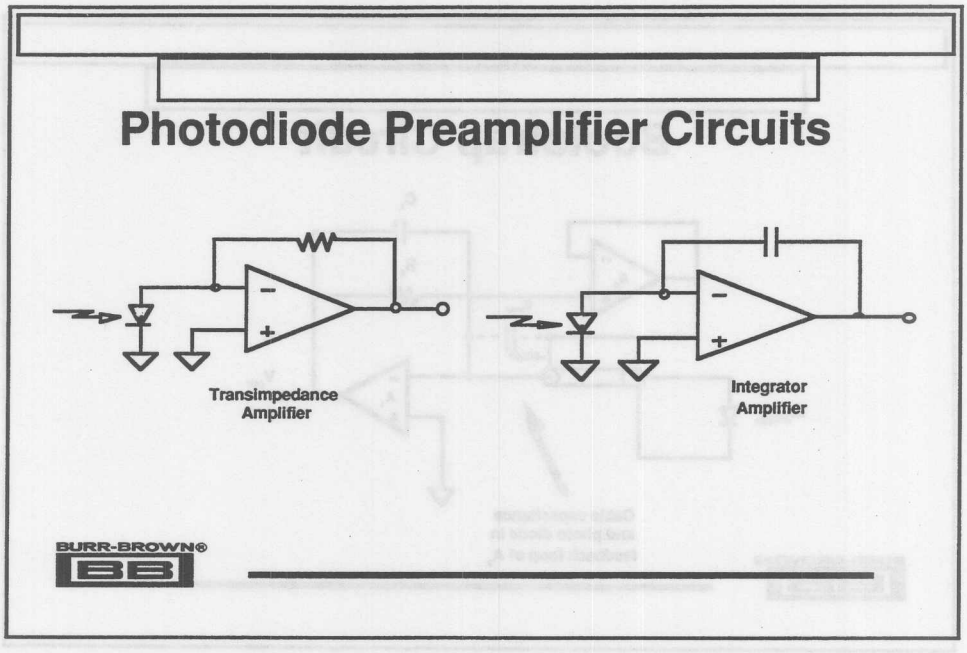
Remote Sensing

In this application, the sensing device is at a remote sight, consequently a coax cable is used to shield the signal line. Unfortunately, the cable has parasitic capacitance of about 500pF, which is place directly across the input of the amplifier. The noise gain at higher frequencies becomes fairly large unless C_2 is also increased. If C_2 is increased, the design trade-off is a decreased signal bandwidth which may not be acceptable.



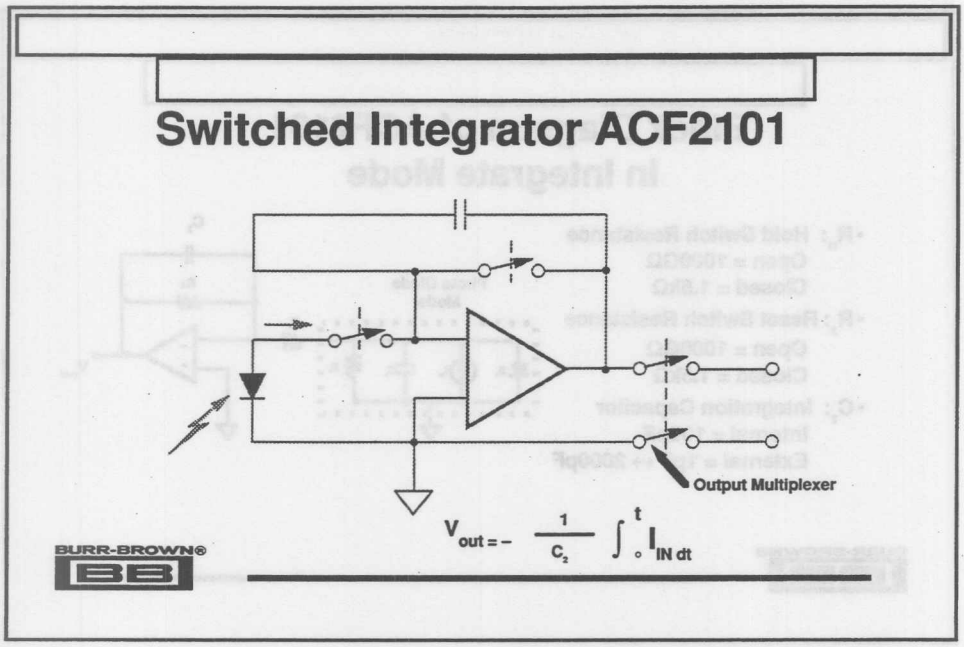
Bootstrap Circuit

A bootstrap circuit can be used to correct this problem. The unity gain buffer, A_2 is added to drive the cable capacitance and remove it from the input of the transimpedance amplifier. A_2 must be carefully selected to have a much wider bandwidth than A_1. The bootstrap amplifier, A_2, may also introduce errors because of its input bias current and noise.



Photodiode Preamplifier Circuits

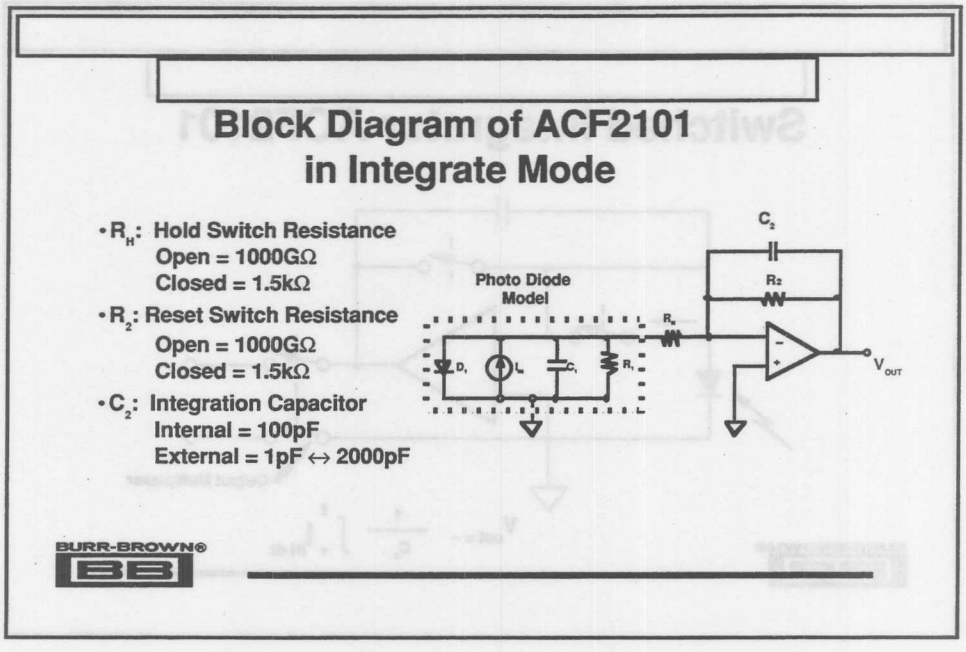
We have been discussing the performance of the transimpedance amplifier, which converts the current of the photodiode to a voltage by use of a resistor in the feedback loop of an amplifier. The integrator amplifier converts the current of the photodiode to a voltage by use of a capacitor in the feedback loop of the amplifier.



Switched Integrator ACF2101

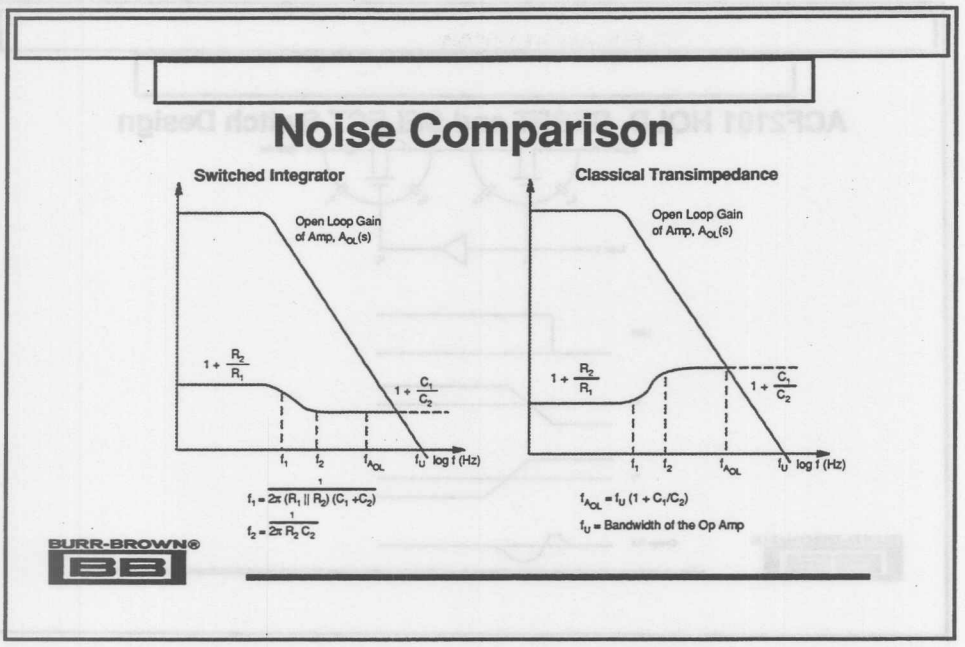
The integrator amplifier requires switches to properly perform photodiode sensing. If the HOLD switch is closed, the input current charges the capacitor in the feedback loop of the amplifier. Since the inverting input of the op amp is held at a virtual ground potential, the output of the amplifier changes in a negative direction over time. The transfer function of the switched integrator is dominated by the integration capacitor and time.

If the HOLD switch is opened, the photodiode current, Iin, is disconnected from the input of the amplifier and the output of the op amp will stop changing. The SELECT switch allows the user to multiplex the output of the switched integrator to a bus. Once the output voltage of the integrator is read, the RESET switch is closed and the output of the amplifier returns to ground, ready for the next integration cycle.



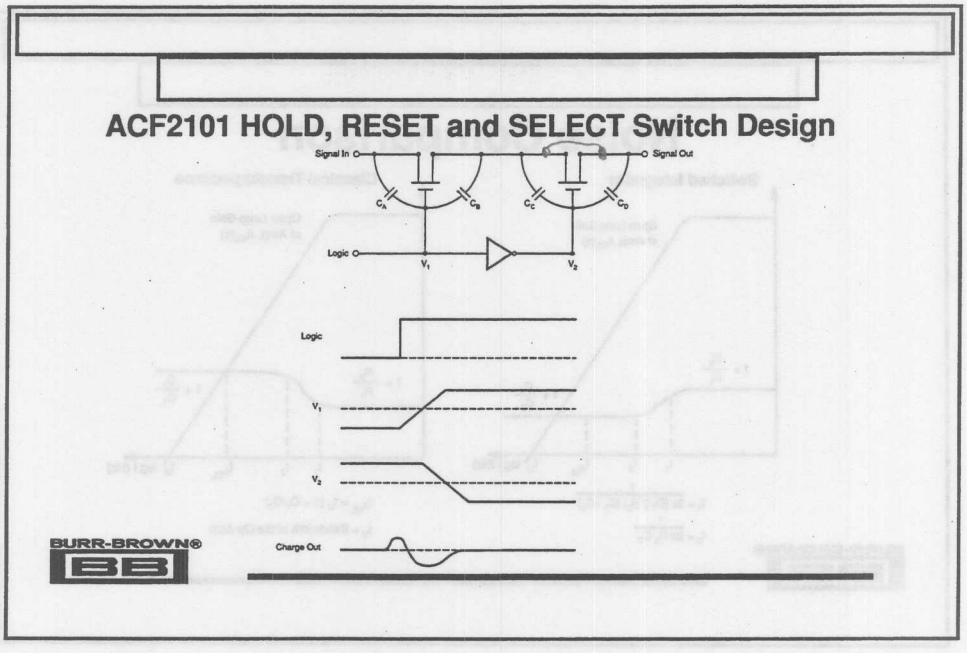
Block Diagram of ACF2101 in Integrate Mode

The switched integrator can be modelled with the same circuit that the classical transimpedance amplifier was modelled with. The photodiode is shown here as an ideal diode, a current source and an R/C pair. R_H models the resistance of the HOLD switch. When the HOLD switch is closed the equivalent resistance across the switch is 1.5kΩ. R_2 models the resistance of the RESET switch. The RESET switch is opened during most of the integration cycle. In the noise evaluation of the circuit, the RESET switch is assumed to be opened and equal to 1000GΩ. The integration capacitor, C_2, is included on the ACF2101 chip and equal to 100pF. This capacitor is trimmed to within ±2pF. An external capacitor can be used instead. The noise performance of the amplifier in the ACF2101 dual switched integrator is similar to the OPA111 noise performance.



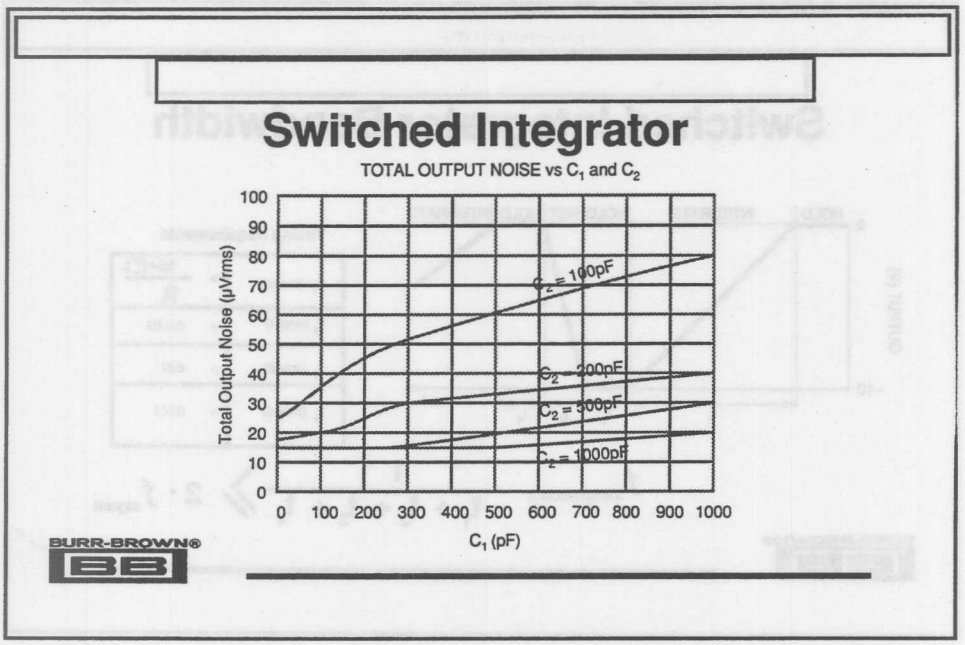
Noise Comparison

Plots showing the noise gain of the switched integrator circuit is compared to the classical transimpedance amplifier noise gain. The zero, f_1, occurs at approximately the same frequency for both plots. The pole, f_2, for the switched integrator occurs at a very low frequency, where in the transimpedance amplifier f_2 occurs at higher frequencies. Both the switched integrator and the transimpedance amplifier total noise is dominated by noise gain at the higher frequencies for the same reasons previously discussed. Consequently, the noise contribution of the op amp in the switched integrator circuit is equal to the noise of the amplifier times the gain of the input and output capacitors, C_1 and C_2.



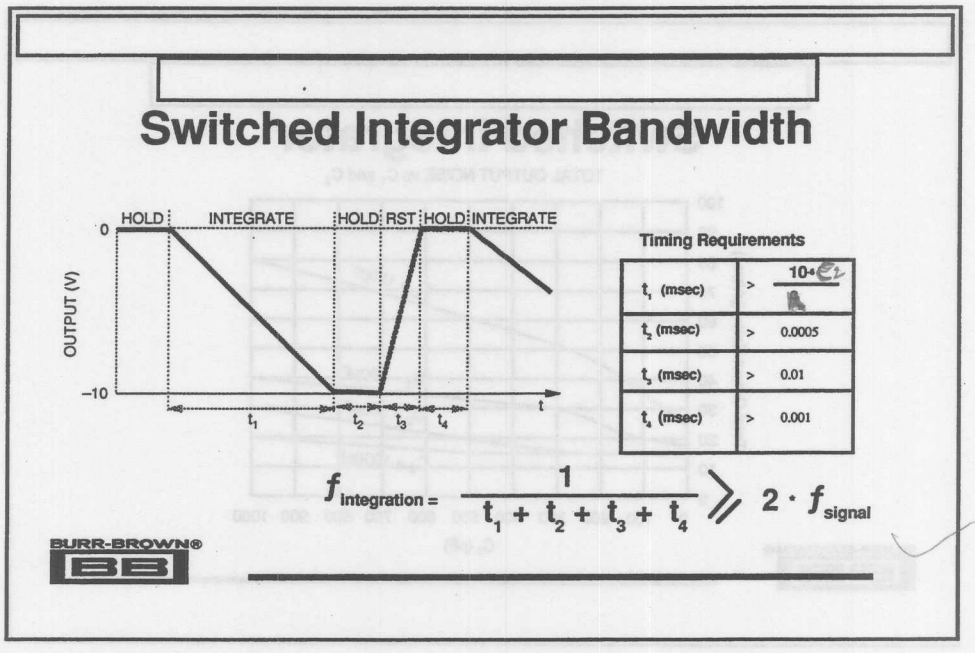
ACF2101 HOLD, RESET and SELECT Switch Design

In addition to the gained op amp noise, charge injection and capacitor noise, KT/C, also contribute to the total noise figure of the switched integrator. The ACF2101 HOLD, RESET and SELECT switch design that is shown here reduces charge injection noise. As illustrated, when the LOGIC node changes from low to high, the voltage change across the capacitors CA and CB pull charge out of the SIGNAL IN and SIGNAL OUT nodes. The inverted LOGIC signal at V2 pushes an equal amount of charge through CC and CD back into the SIGNAL IN and SIGNAL OUT nodes. If parasitic capacitors CA,B,C and D are carefully matched, the total charge injection error caused by the LOGIC switching is near zero.



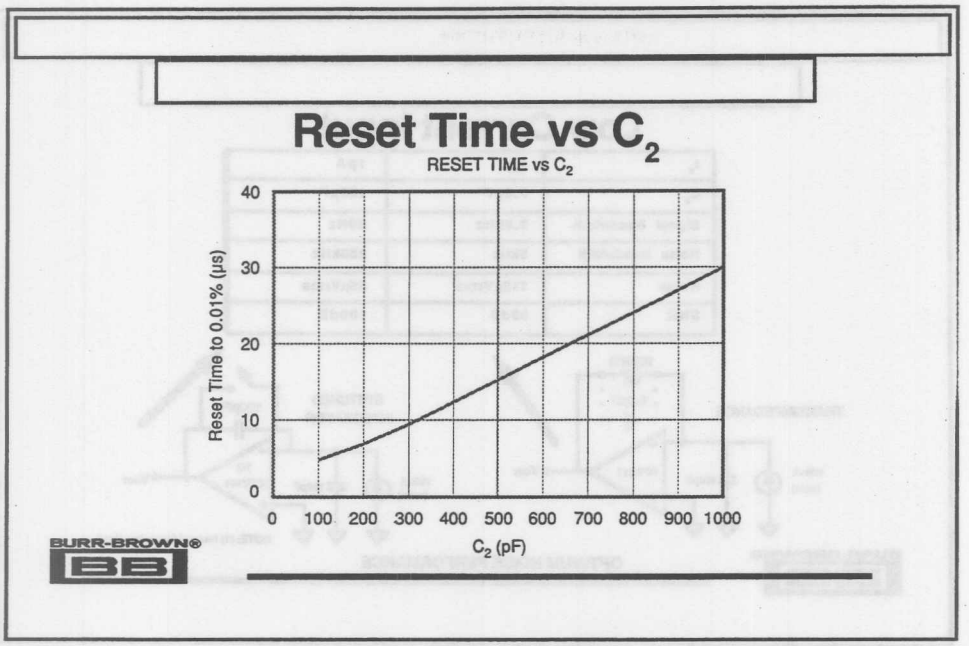
Switched Integrator

The total output noise of the switched integrator is shown in this graph. As expected the output noise increases with increased input capacitance, C_1, and decreases with increased feedback capacitance, C_2. At first glance, the switched integrator looks like the perfect solution for a low noise current-to-voltage converter.



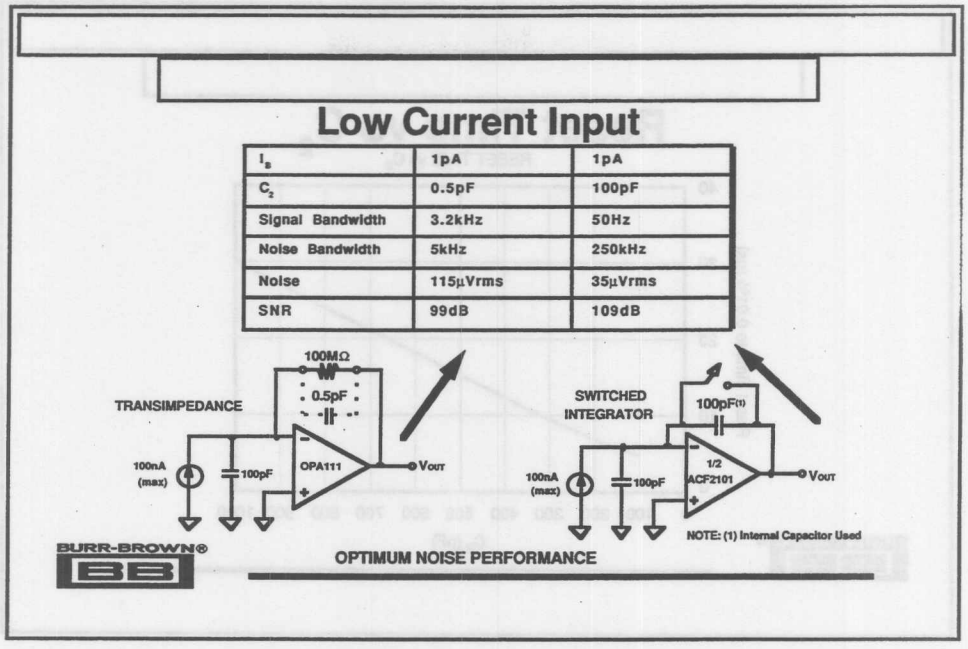
Switched Integrator Bandwidth

The bandwidth of the switched integrator is determined by four regions in the timing diagram. t_1 represents the amount of time required for the output of the amplifier to integrate from zero volts to full scale. The amplifier slew rate is 1V/µs, which limits the minimum integration speed. t_2 represents the amount of time required to open the HOLD switch and read the output of the amplifier. The HOLD switch requires a minimum of 500ns to open. t_3 represents the amount of time required for the output of the amplifier to change from full scale -10 volts to zero. This time is limited by the speed of the time constant R_2 and C_2 in the feedback loop of the amplifier. In this case R_2 is equal to 1.5kΩ because the RESET switch is closed. t_4 represents the amount of time required to close the HOLD switch and restart the integrate cycle. As these times increase, the bandwidth of the switched integrator will decrease.



Reset Time vs C_2

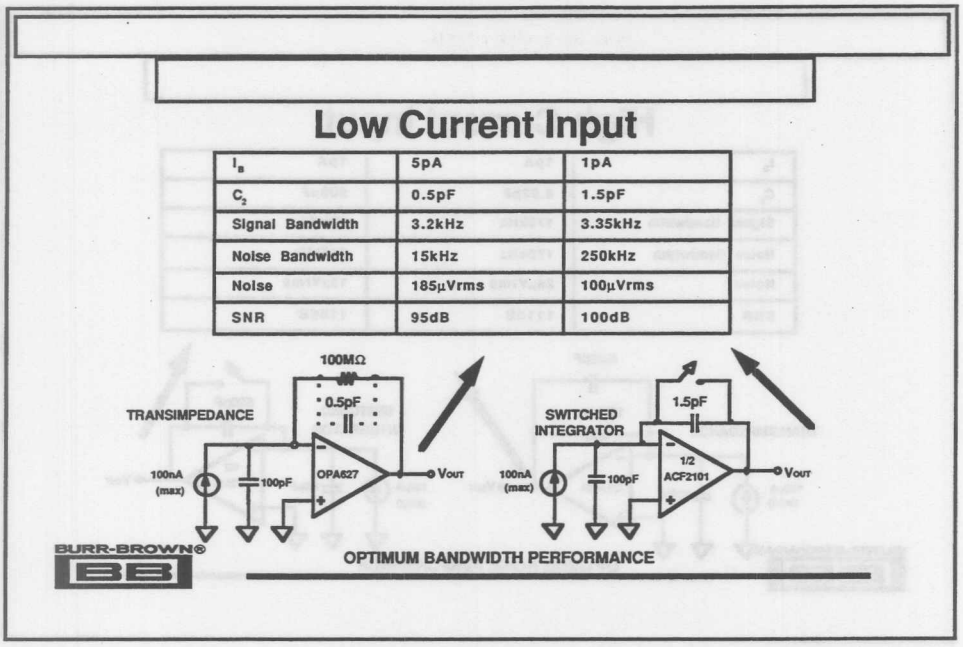
The RESET time, or t_3 and its relationship to the feedback capacitor C_2 is shown here. As the integration capacitor is increased, the reset time is also increased. This timing relationship is usually misunderstood and overlooked. If the reset switch is opened too early, the output will not start at zero for the next integration. Also keep in mind that C_2 does affect the noise performance of the circuit. As a general rule, an increase in C_2 reduces the total noise of the switched integrator, and in some cases can also reduce the signal bandwidth due to the increase in the time to reset the output of the amplifier.



Low Current Input

For comparison, a transimpedance amplifier and switched integrator amplifier are both optimized for low noise performance. In this example, the input diode has a parasitic capacitance, C_1, equal to 100pF and a full scale output current of 100nA.

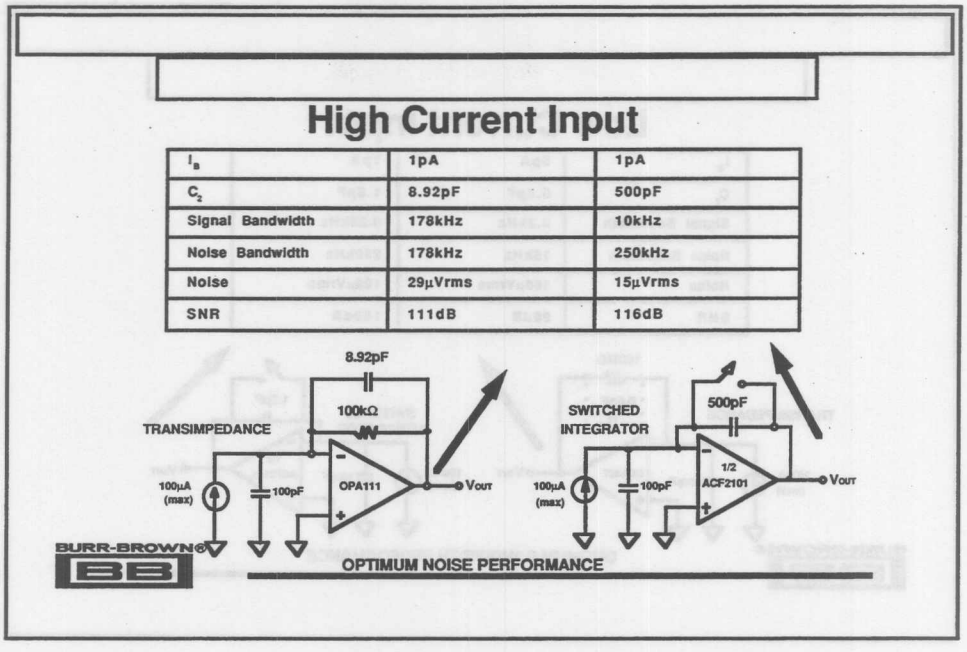
The OPA111 is used as the amplifier in the transimpedance circuit. Notice that the signal-to-noise ratio of the switched integrator is far superior, however, the bandwidth of the switched integrator may not be acceptable at 50Hz.



Low Current Input

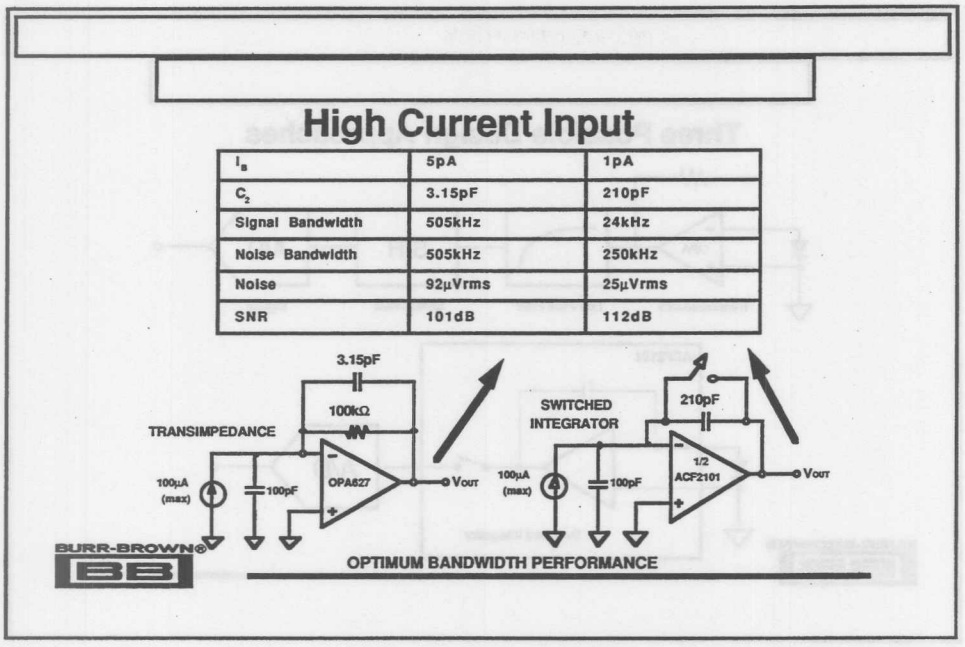
The same input conditions are used again and the transimpedance amplifier and switched integrator are optimized for bandwidth. In this example, the OPA627 is chosen because it is a wide bandwidth FET op amp compared to the OPA111. The signal bandwidth of the circuit does not improve from the circuit with the OPA111 because the parasitic capacitance of the feedback resistor, R_2. On the other hand, the switched integrator can obtain the same bandwidth with a better signal-to-noise ratio.

The switched integrator is the better of the two design approaches for low level input currents.



High Current Input

In this example, the input diode has the same input capacitance as in the previous example, but a full scale output current of 100μA. The OPA111 is again selected as the preferred op amp for the transimpedance circuit. In this instance the signal-to-noise performance of the switched integrator is superior to the transimpedance amplifer.

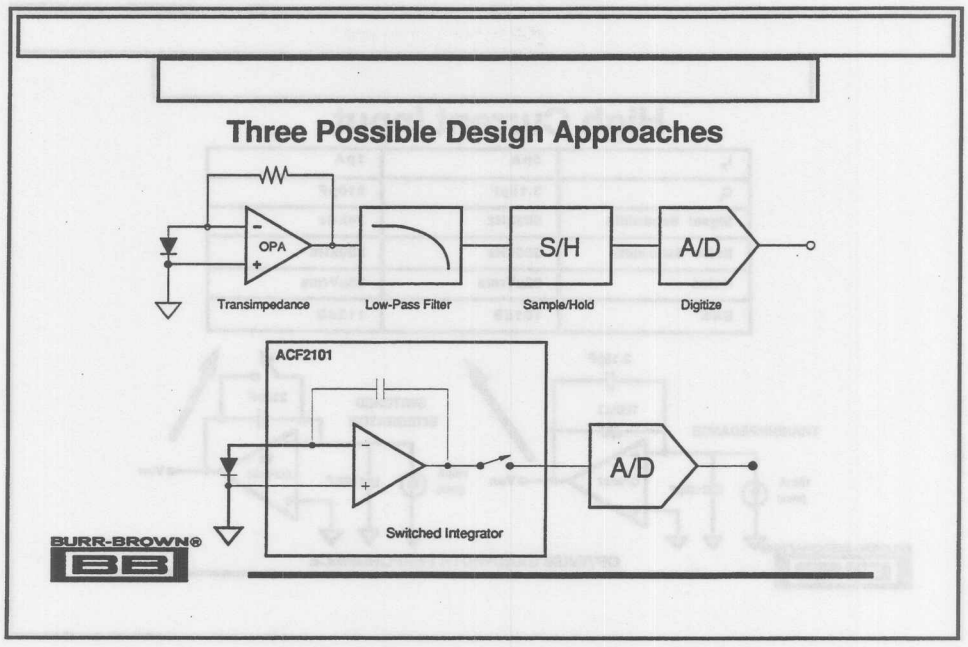


High Current Input

The transimpedance amplifier circuit is now optimized for bandwidth with the OPA627. The noise increases slightly, but the bandwidth performance is much improved. The switched integrator bandwidth also improves slightly with a slight increase in noise.

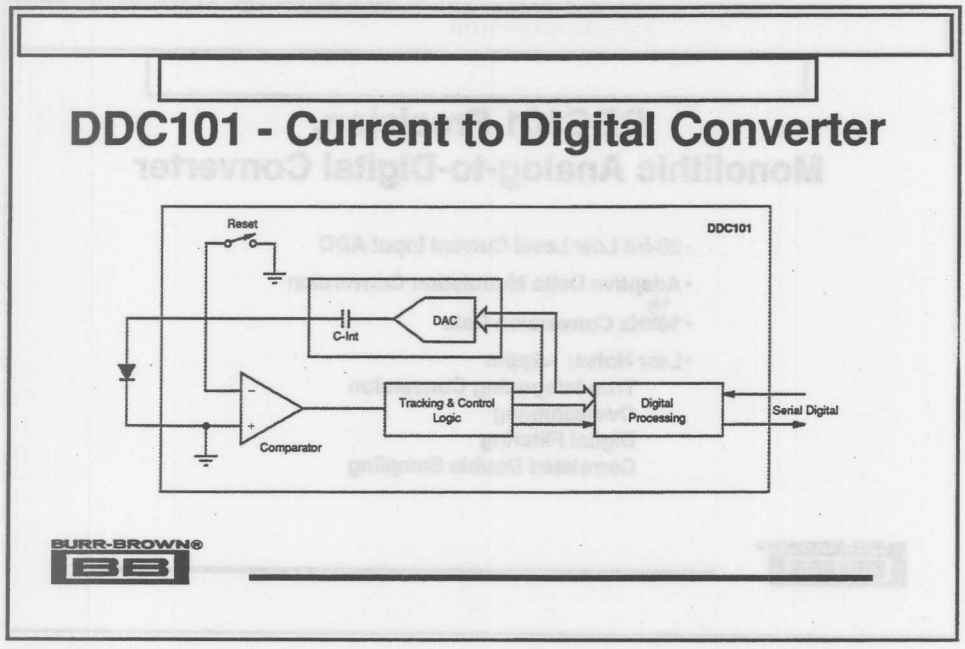
This noise comparison is slightly misleading. If the noise bandwidth of the transimpedance amplifier is reduced to the same signal bandwidth as the switched integrator, the transimpedance noise is 6.5μVrms giving a signal-to-noise ratio of 124dB for the transimpedance amplifier! This reduction in bandwidth is easily done with a unity gain filter at the output of the transimpedance amplifier.

In conclusion, in instances where the photodiode has a high maximum output current, the transimpedance amplifier will give better noise and bandwidth performance.



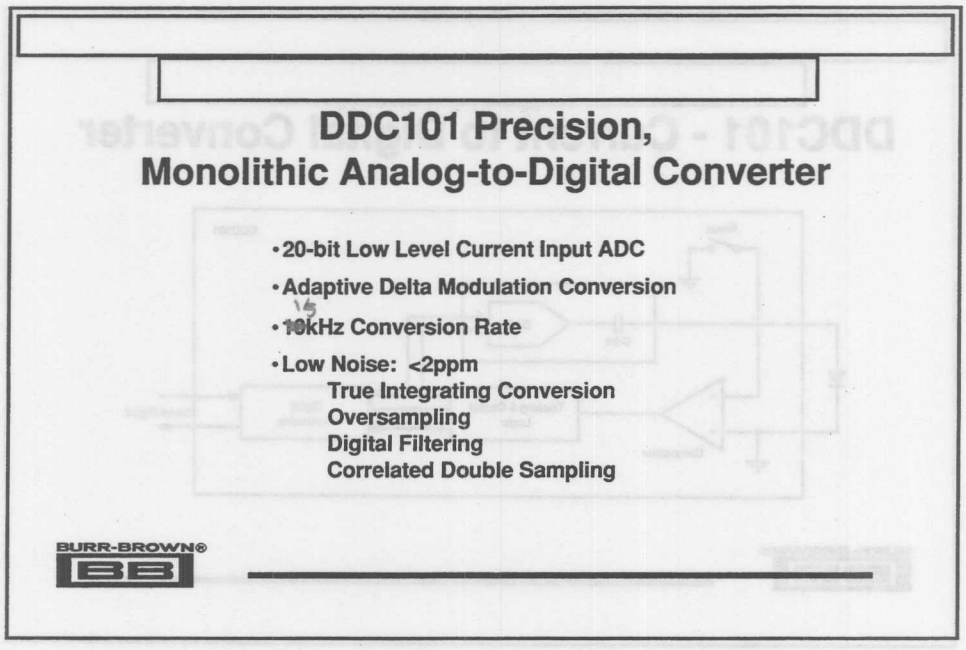
Three Possible Design Approaches

The two design approaches that have been discussed today have been the classical transimpedance amplifier and the switched integrator. The transimpedance amplifier is usually followed by a low-pass filter to reduce the noise, then a Sample/Hold circuit and finally digitized with and A-to-D converter. The switched integrator incorporates the low-pass filter and sample/hold into its overall function by use of an averaging transfer function and the switching network. The output of the switched integrator can be immediately digitized if desired.



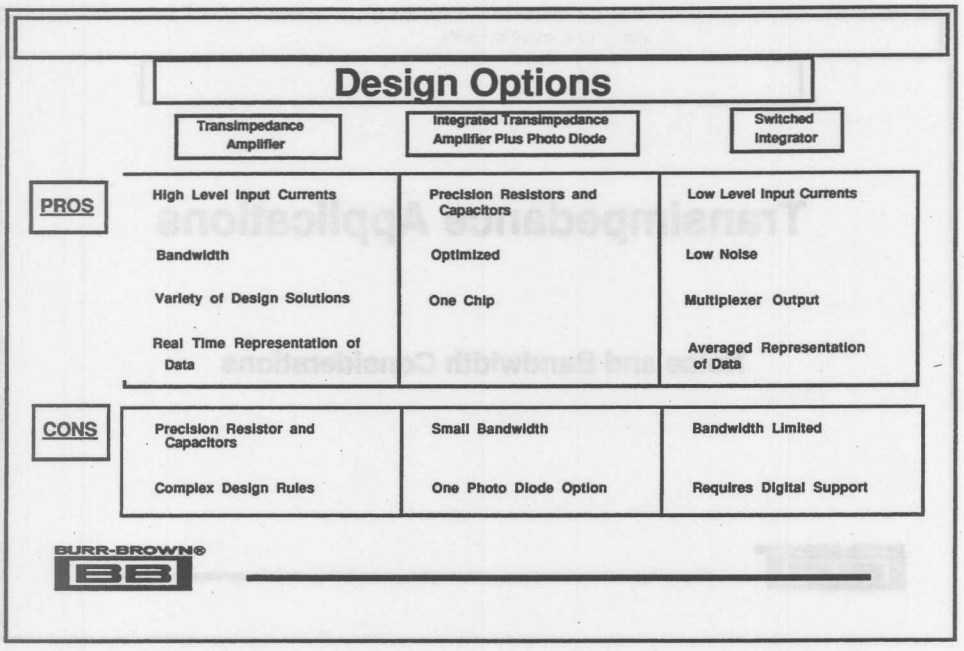
DDC101 - Current to Digital Converter

A third design approach not yet discussed in this seminar is the integrated current to digital convertter shown here. This precision, low-level input current A/D converter is optimized to convert current to a serial digital output eliminating errors that are found in discrete designs. The DDC101, integrates and directly digitizes a photodiode current.



DDC101 Precision, Monolithic Analog-to-Digital Converter

The DDC101 is a precision, wide dynamic range, charge digitizing, A to D converter, that directly accepts low level input currents. Our patented delta modulation topology combines the traditional functions of current-to-voltage conversion, programmable gain, A/D conversion and digital filtering. The maximum conversion rate is 15kHz or a minimum integration time of 100μ seconds. The DDC101 is optimized for low noise operation. We have used an number of techniques to optimize the low noise, such as, integrating the signal, oversampling, digital filtering and correlated double sampling.



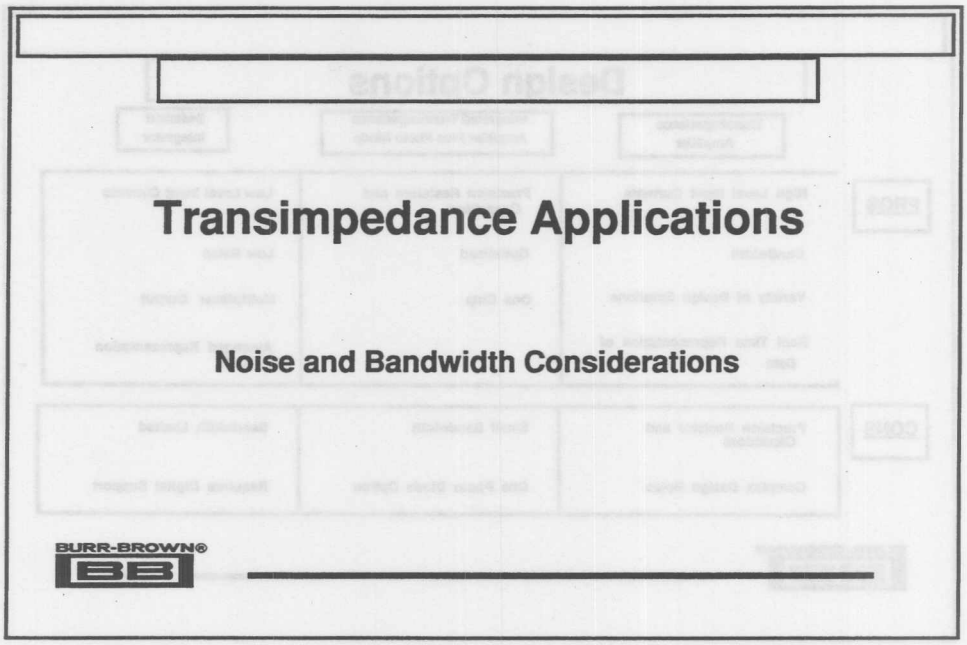
Design Options

The classical transimpedance amplifier has advantages such as a real time representation of the data and wider bandwidth capability, however, the selection of precision resistors and capacitors is difficult particularly in a manufacturing environment. The transimpedance amplifier is most easily optimized for high level input currents from the photodiode.

The integrated transimpedance amplifier plus the photodiode, or the OPT201 solves many of the design problems of the classical transimpedance amplifier, but has a limited bandwidth. The OPT201 is an integrated solution, consequently, the resistors and capacitors on the chip are precise and the transimpedance design has been optimized.

The switched integrator solution provides a averaged representation of the input signal and a multiplexer on the output of the device. The bandwidth is limited and digital circuitry support is required in the design. The noise and bandwidth performance can be superior to the classical transimpedance approach with low level input currents.

No one solution is right for all applications. The choice should be made based on the application input and output requirements.



Transimpedance Applications

This concludes the section covering low level current-to-voltage conversion applications. Are there any questions.

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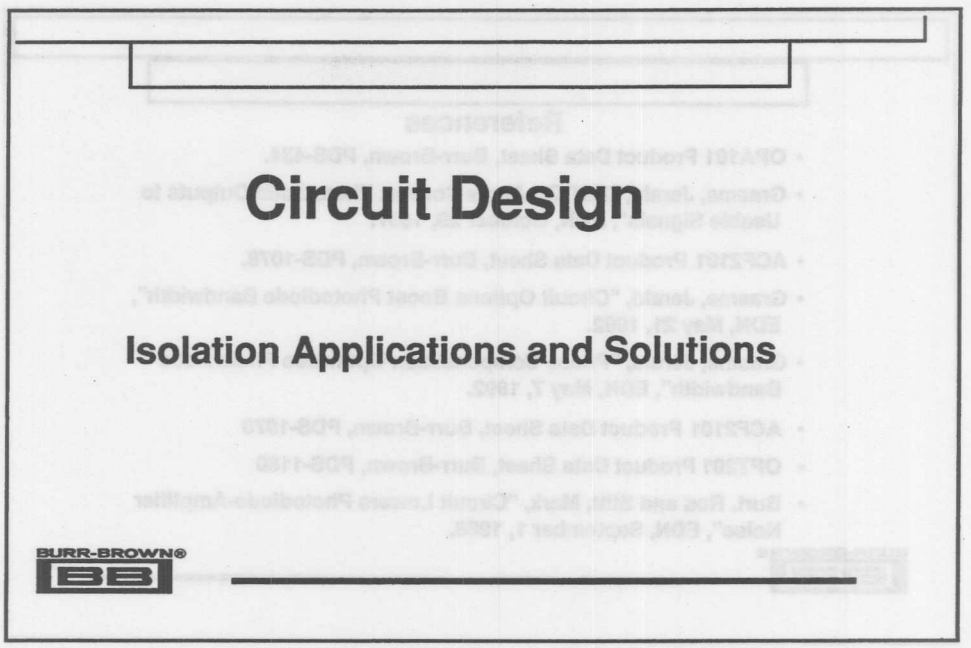
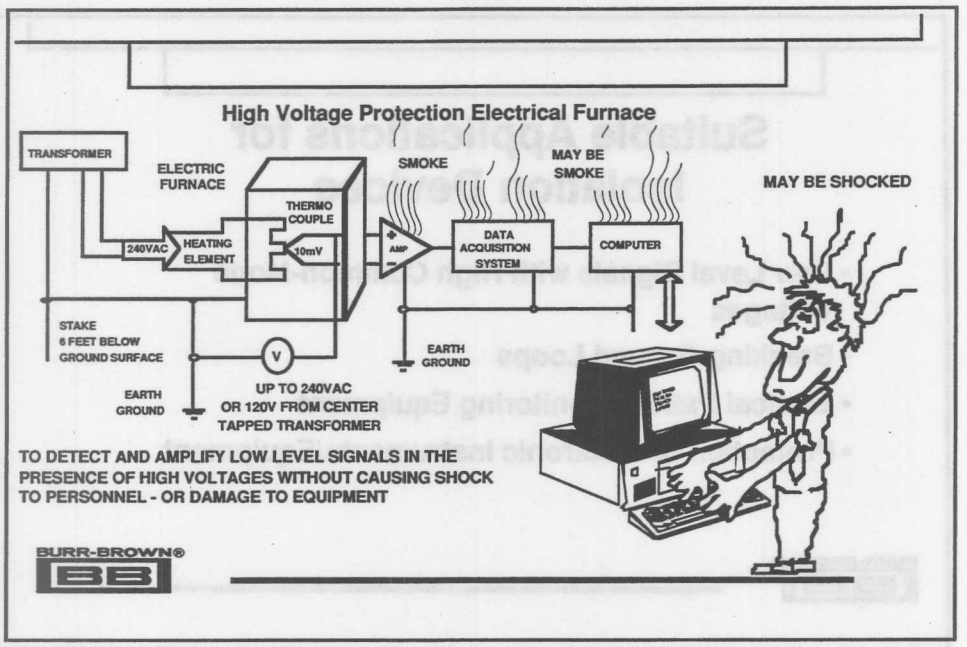


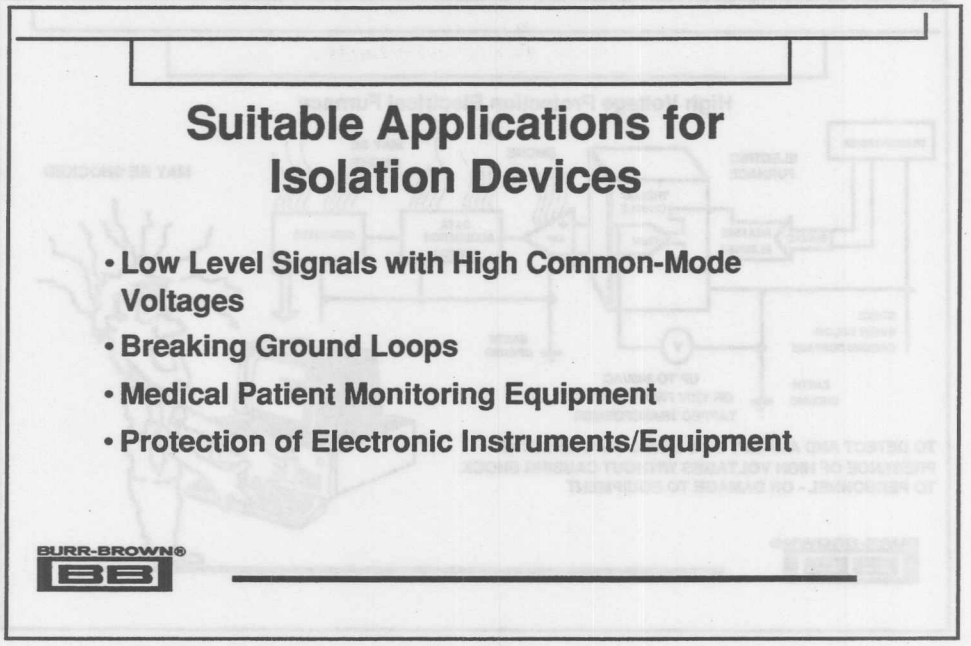
Circuit Design

An isolation device has the primary function of providing galvanic isolation between the input signal and the output signal.



High Voltage Protection Electrical Furnace

Isolation amplifiers and couplers act as an interface between remote sensors, motors, and data acquisition systems, where low signal levels are detected and amplified. In the presence of high voltages, isolation devices provide galvanic isolation between the input and output potentials so to prevent personnel or equipment damage. Here galvanic isolation means that there is a break in the ohmic continuity of the electrical signal. Various types of fields are used to transmit the electrical signals across isolation barriers, such as a B-field in the case of an inductor, an E-field in the case of a capacitor or a light field in the case of an LED. The galvanic isolation between the input and output potentials of the isolation device allow accurate transmission of signal across a high voltage barrier, avoiding possible cross-coupling or interaction between two or more circuits.



Suitable Applications for Isolation Devices

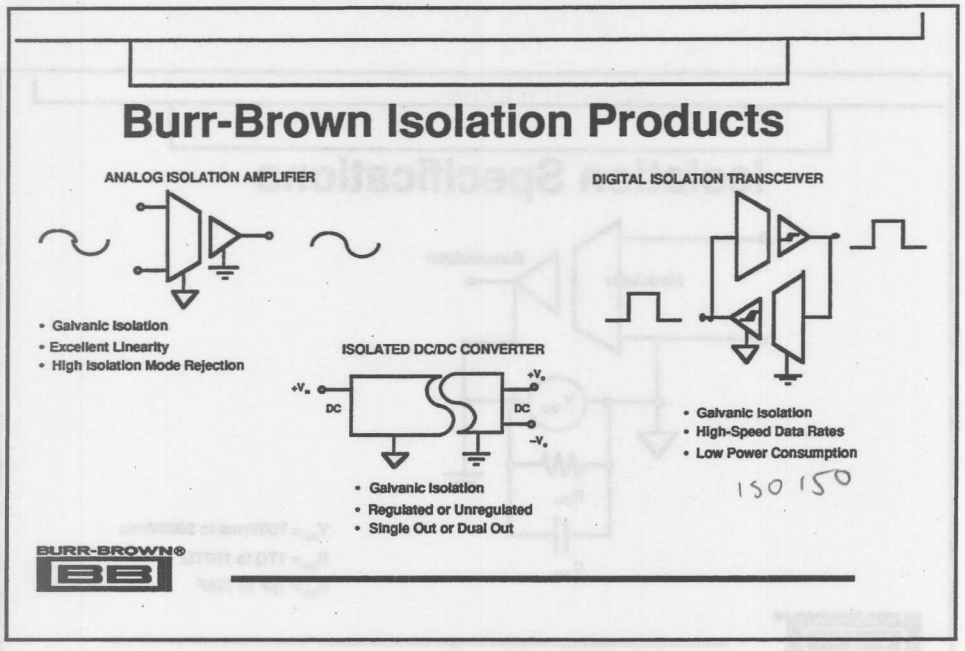
In general, most applications can be broadly categorized in the following four types:

*Amplifying and measuring low level signals in the presence of high common-mode voltages.

*Breaking ground loops or eliminating source ground connections. The isolation device provides full floating input, eliminating the need for connections to source ground, and allowing two-wire hook-up to the signal sources.

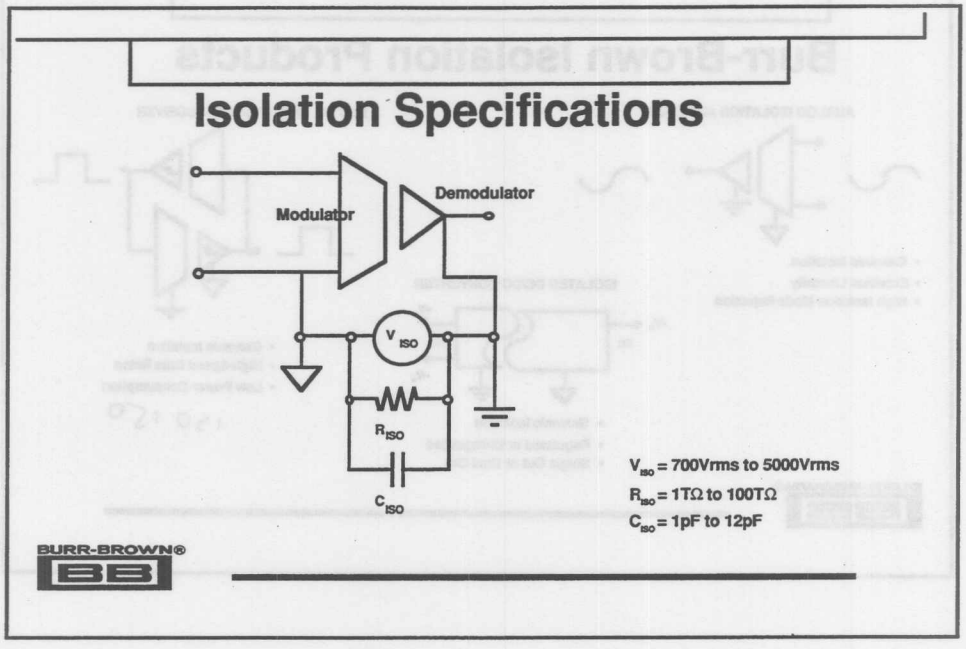
*Providing an interface between medical patient monitoring equipment and the transducer or device that may be in physical contact with the patients. Such applications require high isolation voltage levels and very low leakage currents.

*Providing isolation protection to electronic instruments or equipment. Large common-mode voltages occasionally cause hazardous electronic faults. The low leakage currents and high isolation voltage capability of isolation amplifiers help protect instruments against damage caused by such faults.



Burr-Brown Isolation Products

Signals can be transmitted across a galvanic isolation barrier in the form of analog, digital or DC. Analog isolation amplifiers usually consist of an input operational amplifier followed by a unity-gain isolation stage. The sole purpose of the unity-gain isolation stage is to completely isolate the input from the output of the device. Isolated digital transceivers transmit digital signals at high speed data rates across the isolation barrier with low power consumption. Isolated DC/DC converters are used to power the electronics on the isolated side of the barrier. They are available as regulated units or unregulated with a variety of input and output voltage options. An important feature of these isolation products is that they have completely floating inputs which help eliminate cumbersome connections to source ground.



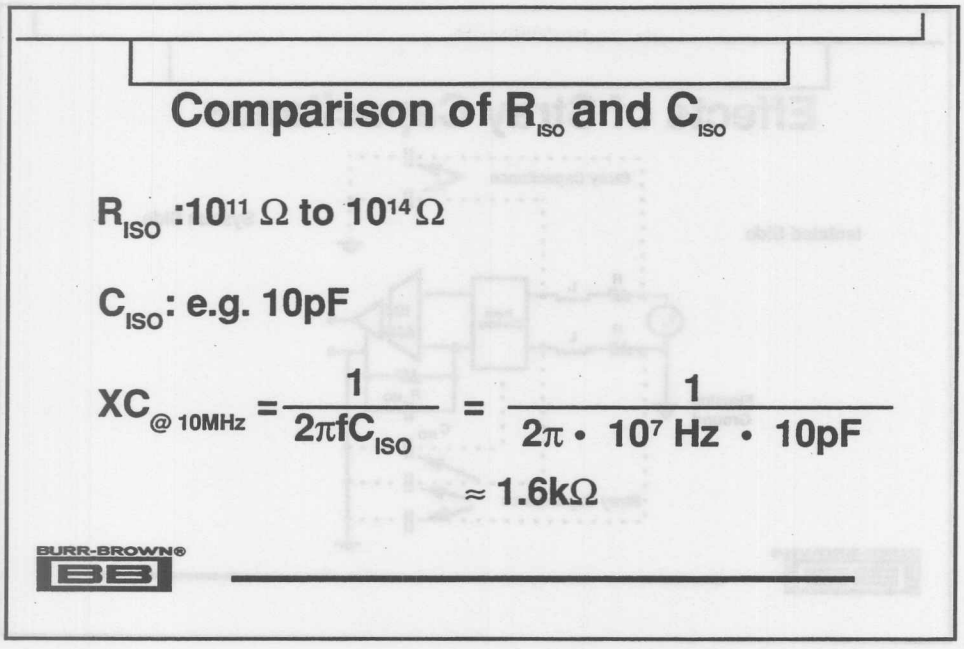
Isolation Specifications

The basic function of isolation amplifiers, digital transceivers and DC/DC converters is like that of their non-isolated counter parts. For instance, an isolation amplifier transmits analog signal from the input to the isolated output of the device. The obvious difference between the isolation amplifier and the standard op amp are the isolation specifications. The barrier of these amplifiers are specified by the isolation voltage, V_{ISO}, parasitic resistance R_{ISO}, and the capacitance C_{ISO}.

V_{ISO} can be selected according to the requirements of the application. Traditionally, the quality of the isolation barrier has been tested by applying a high, 60Hz test voltage and observing increases in the leakage current across the barrier. The test voltage is calculated at two times the continuous isolation voltage rating plus 1000V. The test duration is 60 seconds according to UL544. This test is based on the principle of stress testing.

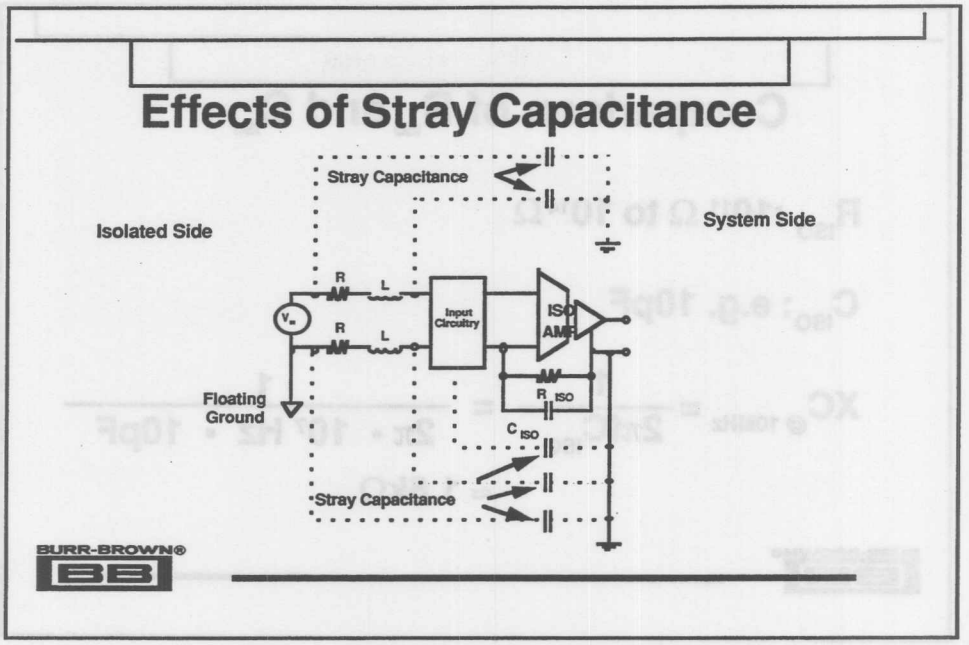
Beginning with the introduction of the capacative coupled isolation amplifiers, new introductions are being tested for partial discharge in accordance with VDE0884. Here a test voltage of 1.6 times the rated isolation voltage of the device is applied across the isolation barrier. Discharge across the barrier up to 4 pC is allowable.

The parasitic capacitance and resistance of the isolation device should be selected to be as low a possible because they form an AC connection between the isolated sides. Although, R_{ISO} is usually in the range of several thousand mega ohms and C_{ISO} is typically less than 10pF, the impedance observed in the RF range is much lower.



Comparison of R_{ISO} and C_{ISO}

Pulse edges of fast computers and switching power supplies generate RF noise. Looking at the example, the stray capacitance is rated at 10pF. The equivalent resistance of that capacitance at 10MHz is as low as 1.6kΩ.

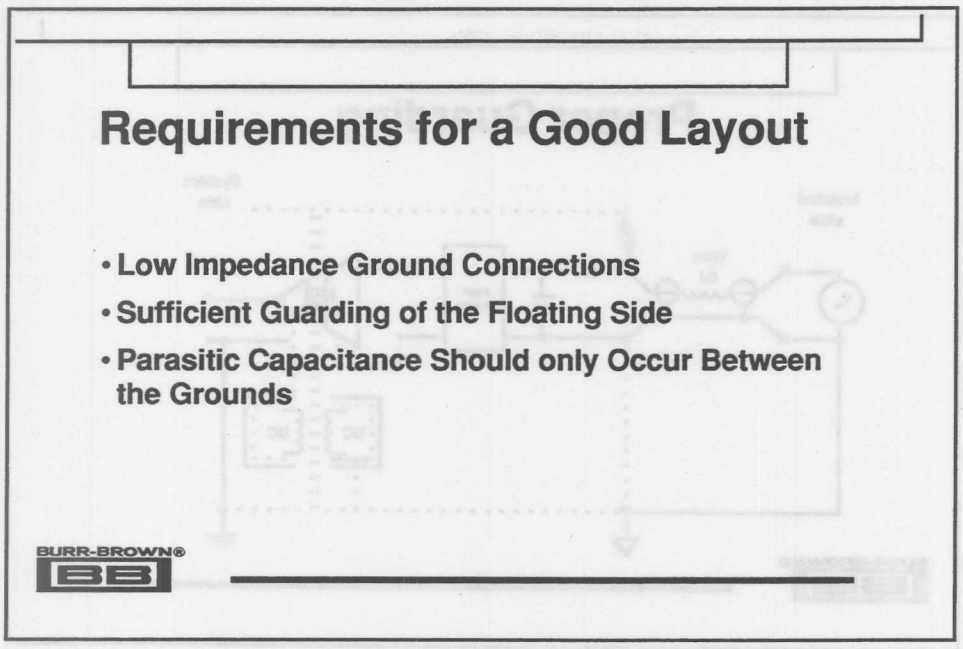


Effects of Stray Capacitance

10pF may seem to be a large value for an isolation amplifier's barrier capacitance, but for a practical circuit board, it's small. One side of the circuit might be DC-referenced to ground, the other side floating. All of the parasitic capacitance from the connectors, components, power supply and connection cables increase the C_{ISO} of the entire circuit.

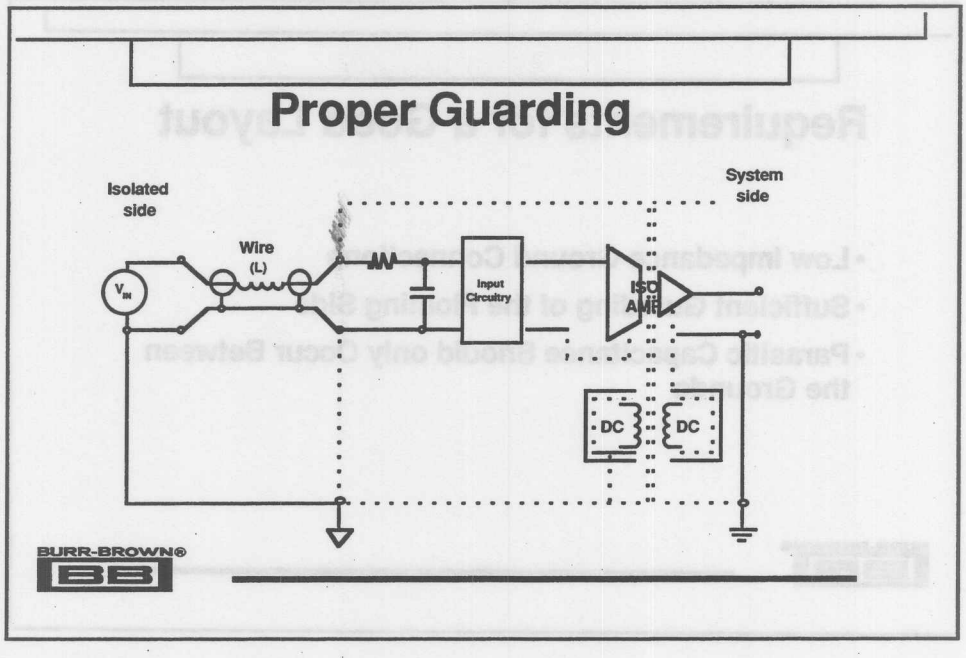
The internal capacitance of the isolation amplifier mainly appears between the input and output ground. Therefore, current generated by changes in the isolation voltage generally flows from one ground to the other. The parasitic capacitors, however, can couple noise directly into the signal path, a factor that should be kept in mind when designing the layout for the circuit.

Capacitive coupling into the floating ground generates current through the ground reference wire. The corresponding voltage drop across the wire resistance and inductance contribute directly to the signal voltage on the input of the isolation amplifier. Since this part of capacitive coupling can not be avoided, a low-impedance ground reference is necessary.



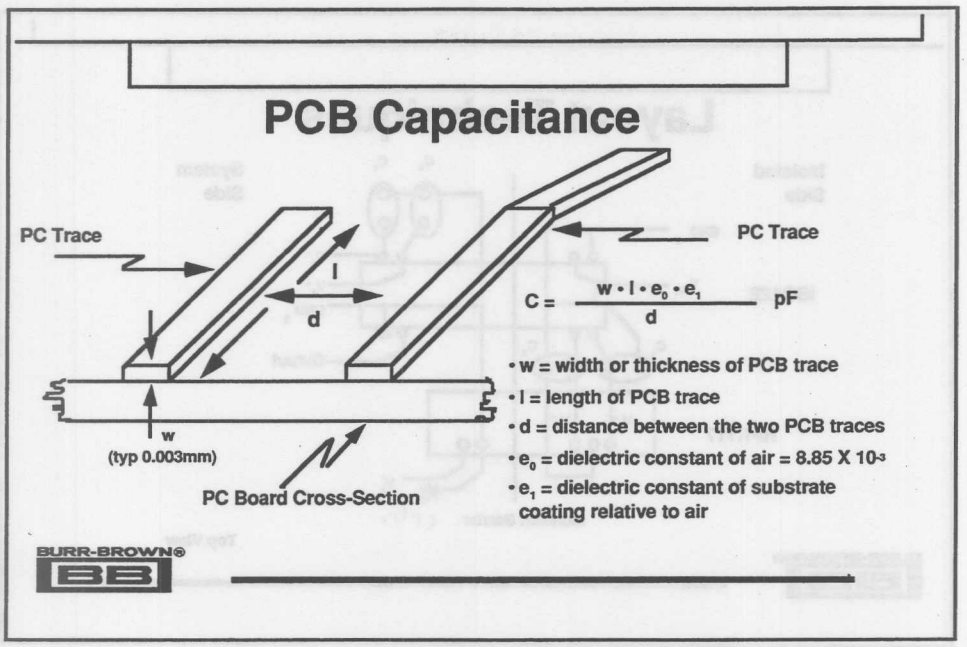
Requirements for a Good Layout

Good layout practices such as low impedance ground connections, sufficient guarding of the floating side and designing the layout so that the parasitic capacitance is between the grounds improve the performance of the circuit.



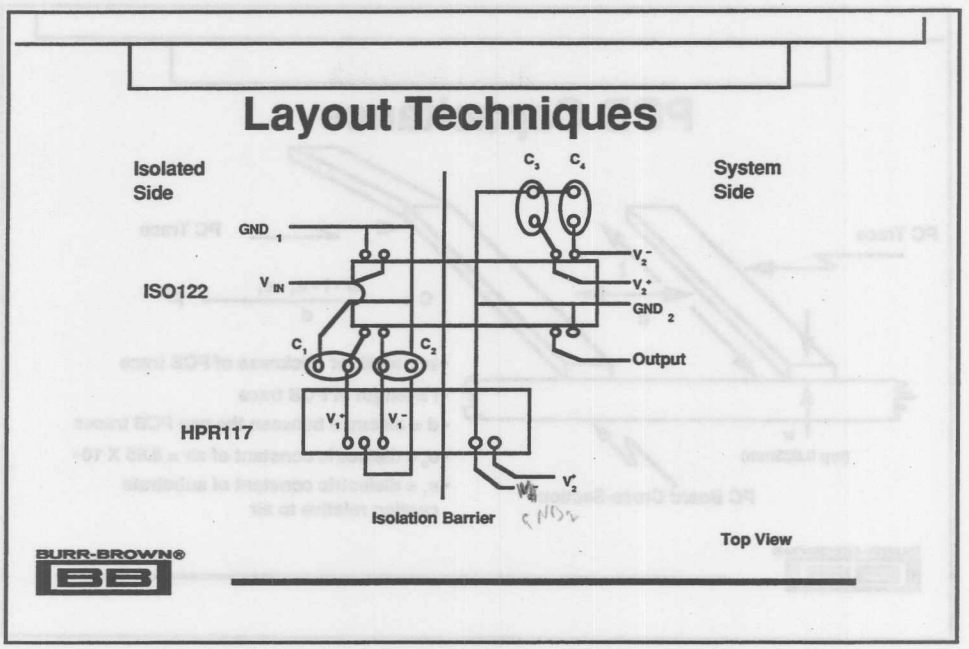
Proper Guarding

Capacitive coupling into components or elements in the signal path generates large errors due to the relatively large noise amplitude. Extensive guarding and a low-impedance circuit design keep this effect small. A low-pass filter at the isolation amplifier's input attenuates current through the sense wire and filters the input voltage.



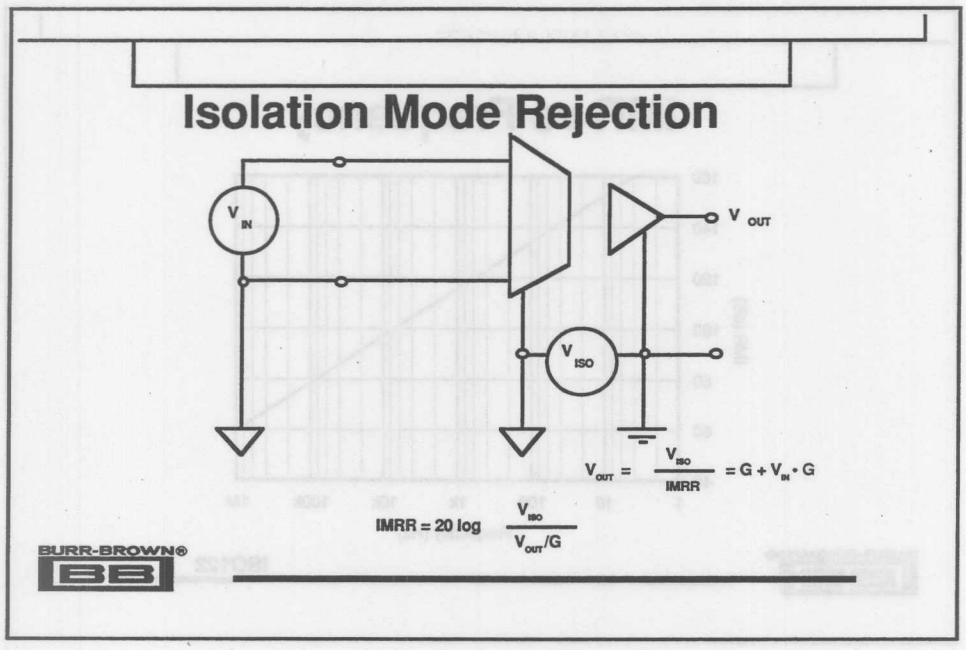
PCB Capacitance

Traces on the PC Board form parasitic capacitors with other traces. The magnitude of the capacitance is dependent on the ratio of the length of the two traces and the distance between them. This first order calculation gives the designer a rough estimate of the stray capacitance that has been designed into the PC Board layout.



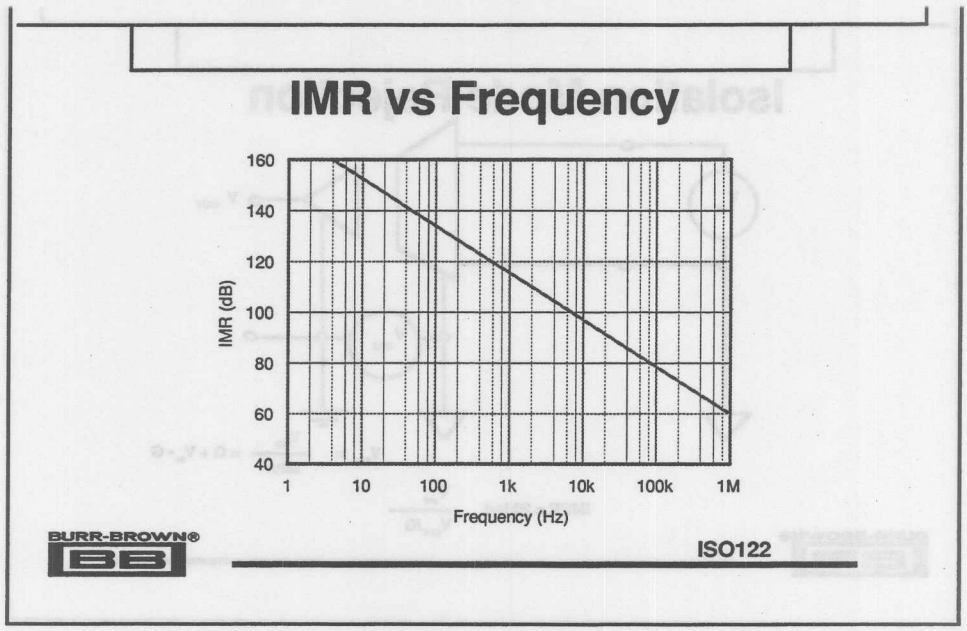
Layout Techniques

Since all parasitic capacitances should only connect ground points, a guard track for the input and output sides is necessary. For example, the signal input pin V_{IN} of the ISO122 lies next to the isolation barrier. In this PC Board layout Ground 1 shields the input from any DC or AC voltages on the system side of the isolation barrier and Ground 2 shields the output of the ISO122 from any noise that could be introduced from the isolated side. High DC or AC voltages can introduce noise into the signal path when the PC Board capacitive coupling can't be avoided.



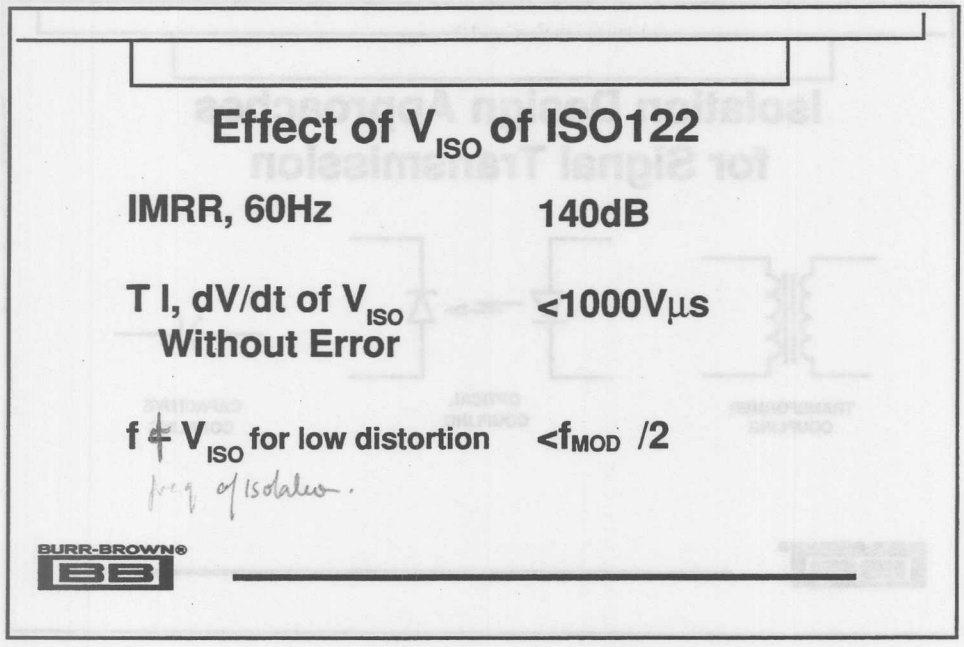
Isolation Mode Rejection

As V_{ISO} increases with amplitude and frequency, guarding techniques become more important. The Isolation Mode Rejection Ratio or IMRR specifies the isolation amplifier's ability to reject the isolation voltage, V_{ISO}. IMRR is the ratio of the isolation mode voltage to the error voltage that appears in the signal path referred to the input.



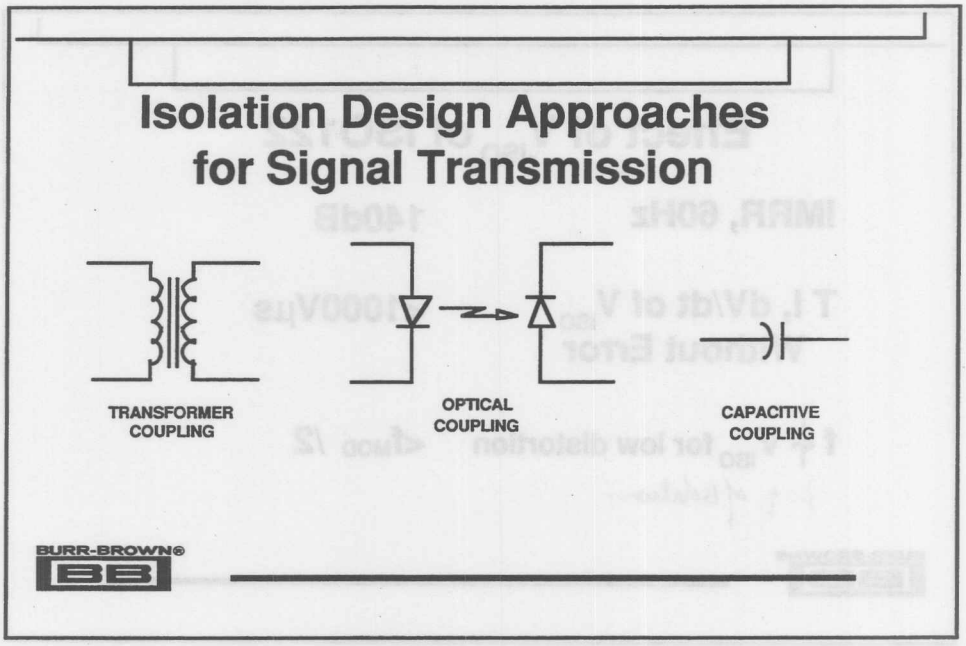
IMR vs Frequency

IMRR ranges from 140dB to 160dB at DC depending on the isolation amplifier. At higher frequencies, however, it decreases 20dB per decade. The isolation mode rejection of the ISO122 is illustrated in the graph. The PC Board layout can degrade this performance dramatically.



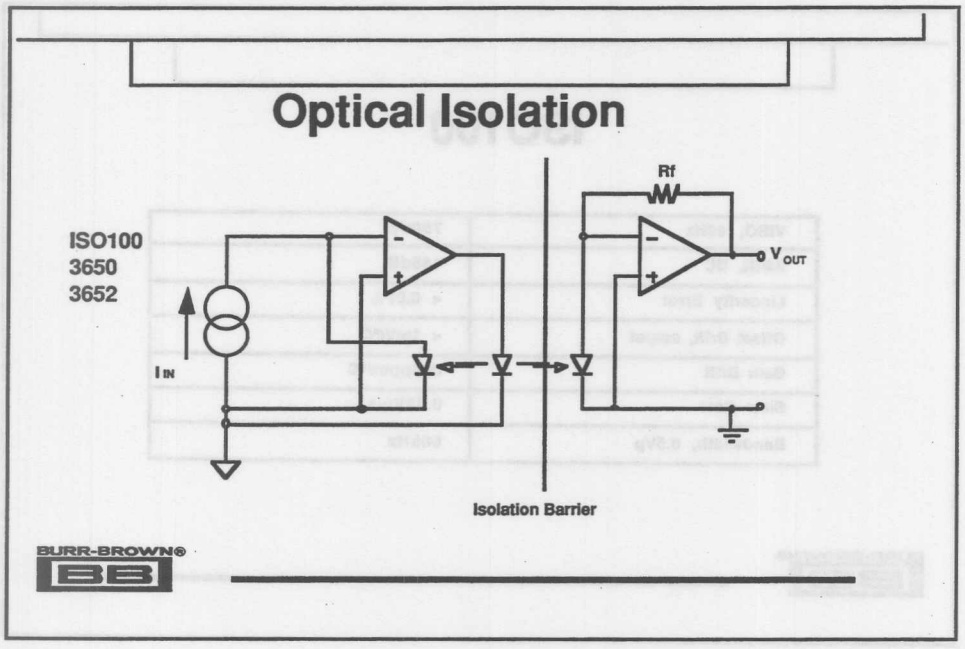
Effect of V_{ISO} of ISO122

Isolation Mode Rejection does not completely describe the sensitivity of the isolation device to RF across the barrier. In particular, steep edges, also known as transients, can overload the amplifier, resulting in nonlinearities, instable offset errors and even saturation effects. The amplifier's ability to reject these transients is specified as Transient Immunity or TI, in the units of Volts per second. In addition, if low distortion is critical, the frequency of the isolation voltage should be less than one half of the modulation frequency of the isolation amplifier.



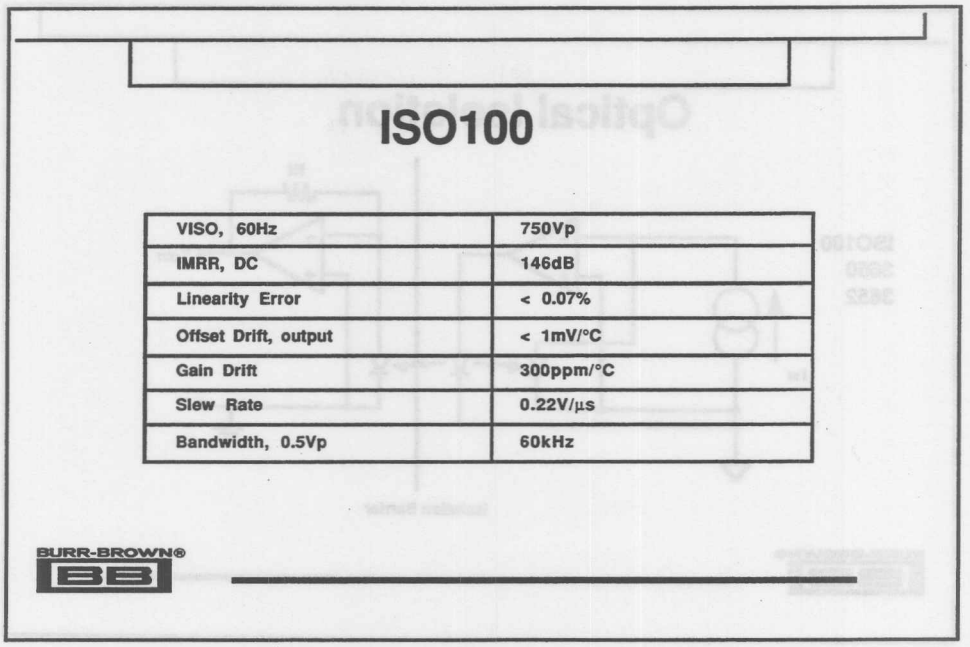
Isolation Design Approaches for Signal Transmission

Three isolation design approaches are used in Burr-Brown's isolation product line to transmit signal across the isolation barrier; optical, transformer, and capacitive. Each design approach offers a set of advantages and disadvantages that should be considered when selecting the isolation device for the application.



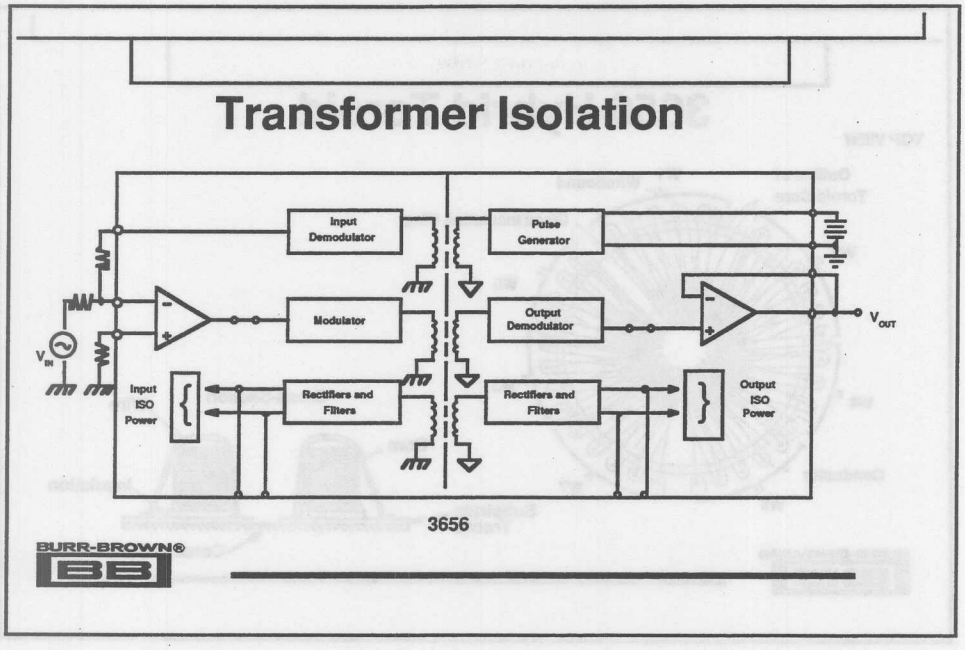
Optical Isolation

Modulating voltage into light is easily done with an LED. Optocouplers use this technique for digital data, but analog signals require a few design tricks to achieve linearity and DC accuracy. The design uses a light control circuit, which senses the intensity in the feedback of the input stage and transmits the same intensity to the output stage. This feedback/feedforward technique compensates for aging and the nonlinearity of the light source.



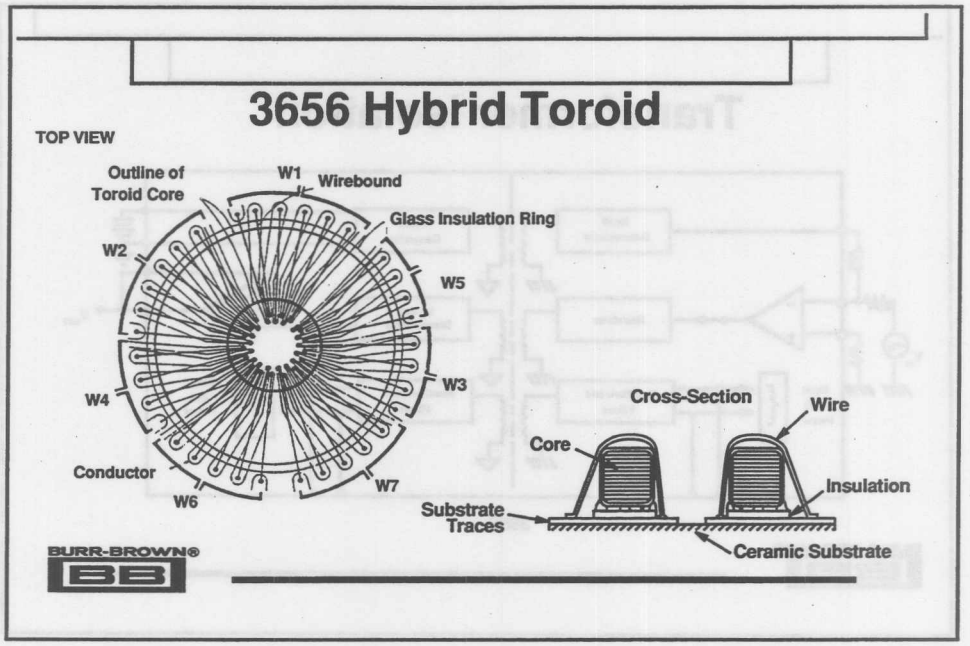
ISO100

This principle can only function if both light receivers are properly matched. As long as this condition is fulfilled, the principle offers real continuous analog signal transmission and is insensitive to interference. It is relatively fast and most importantly, there is no modulation/demodulation ripple voltage generated. These features make the optical isolation amplifier ideal for sensors or sources with high impedance to ground.



Transformer Isolation

The transformer design approach uses a chopper to form an amplitude modulation of the DC signal. The signal is transferred by a transformer and then rectified or demodulated by controlled phase. This technique is relatively tolerant to RF noise; saturation rarely arises, and the signal path recovers quickly after overload conditions.



3656 Hybrid Toroid

The transformer is manufactured as part of the package. In the case of the 3656 isolation amplifier, seven windings are built using a circular magnetic core and wire bond techniques. Here the magnetic core is placed on insulation material to separate the core from substrate traces. The winding around the core is accomplished using wire bonds. One draw back of this design approach is that the signal bandwidth is small.

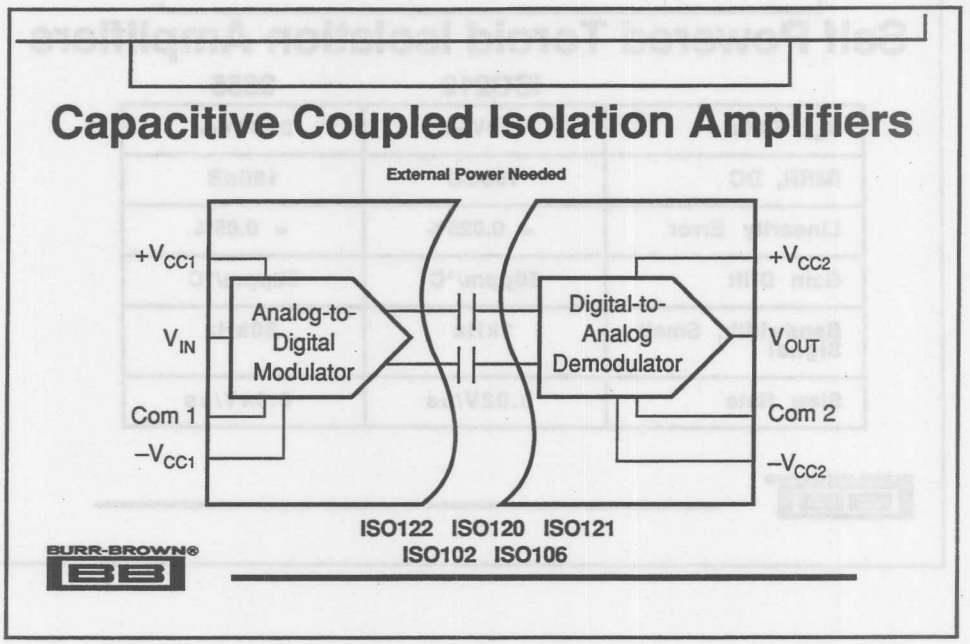
Self Powered Toroid Isolation Amplifiers

	ISO212	3656
V_{iso}, 60Hz	750V_{rms}	2000V_{rms}
IMRR, DC	160dB	160dB
Linearity Error	< 0.025%	< 0.05%
Gain Drift	50ppm/°C	60ppm/°C
Bandwidth, Small Signal	1kHz	30kHz
Slew Rate	0.02V/µs	0.04V/µs

BURR-BROWN®

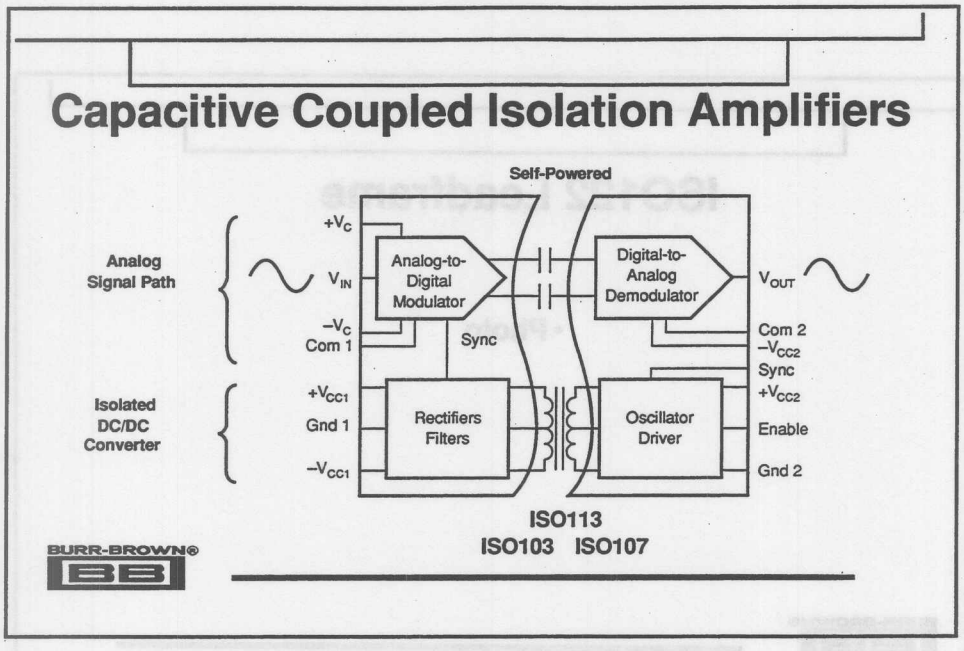
Self Powered Toroid Isolation Amplifiers

Isolation amplifiers using this principle are the 3656 and ISO212. These isolation amplifiers also have DC/DC converters for internal and external power requirements. They work very efficiently in data acquisition systems for DC signals.



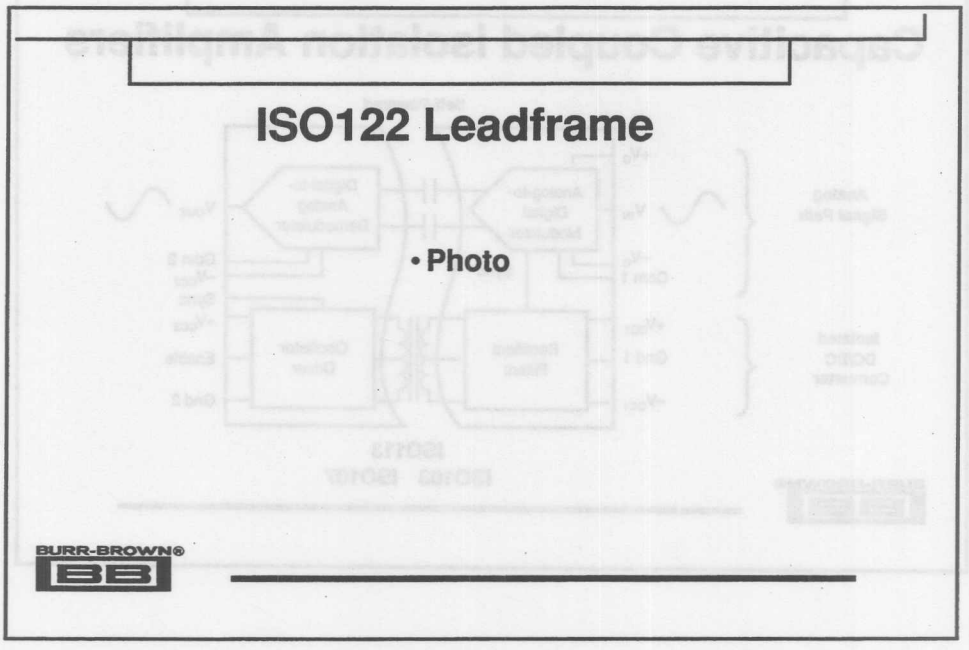
Capacitive Coupled Isolation Amplifiers

Finally, the capacitor design approach uses a duty cycle or frequency modulation technique to transmit the signal across the barrier. The signal is transmitted across the barrier differentially. The output stage receives and demodulates the signal to analog while rejecting common mode signals. Capacitive coupled isolation amplifiers are available with or without a DC/DC converter for internal and external power requirements.



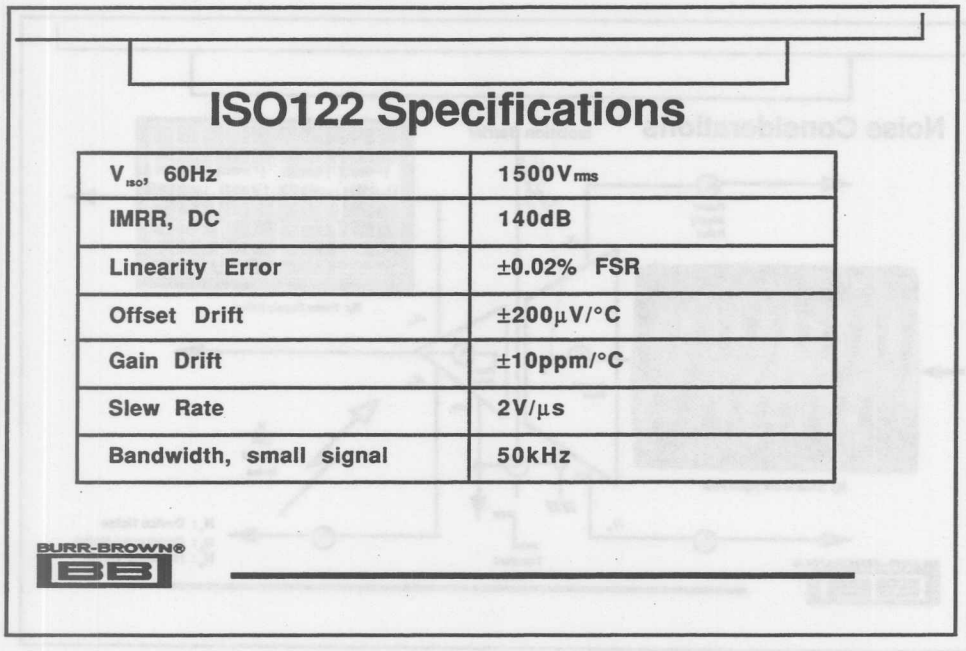
Capacitive Coupled Isolation Amplifiers

The capacitive coupled isolation amplifiers with the DC to DC converter included are synchronizable for multichannel applications. This feature reduces noise in the signal path by reducing the number different oscillator frequencies on the board.



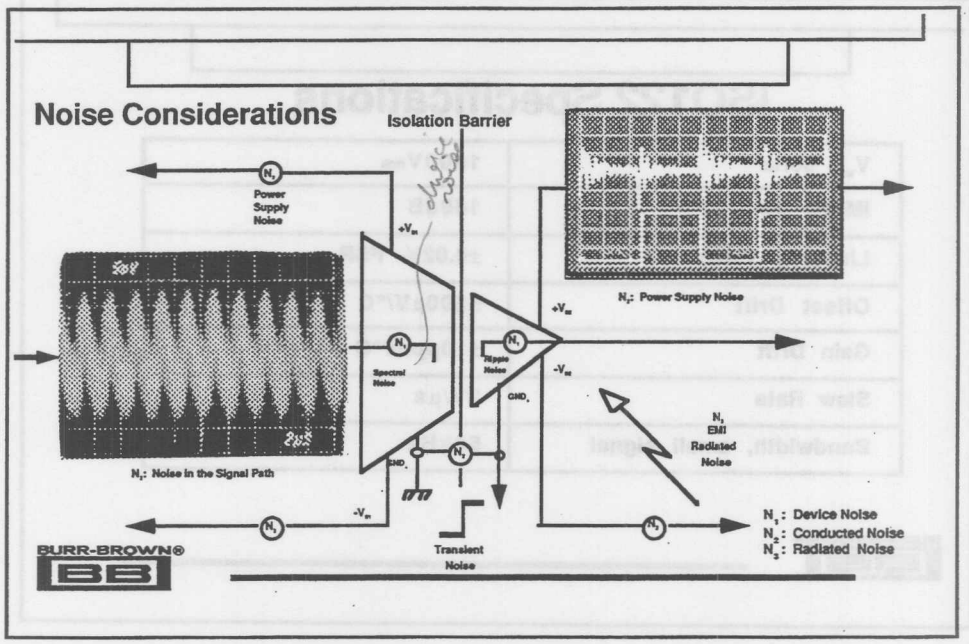
ISO122 Leadframe

The capacitors of these isolation amplifiers are easily built into the package. For instance, the ISO122's isolation barrier capacitors are built using the package leadframe. The transmitter and receiver are monolithic die. This manufacturing technique yields a very cost effective, reliable isolation barrier.



ISO122 Specifications

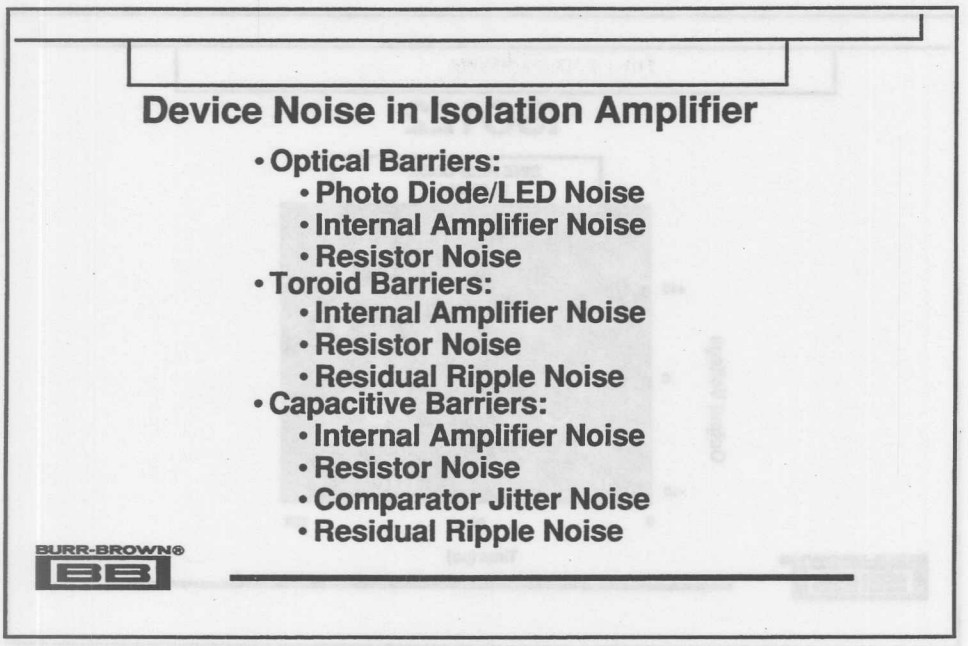
The transmission principle is largely insensitive to isolation mode noise due to the very small capacitance of the couplers. The demodulator only receives the differential pulse edges. Continuous RF interference in the MHz range, however, can interfere with the signal transmission or even overload the receiver, causing a disruption of the signal.



Noise Considerations

Noise is a challenge in any precision application. Design considerations and layout rules many times can reduce the noise figure to tolerable levels. In an environment where isolation is used, the noise sources can be put into three general categories.

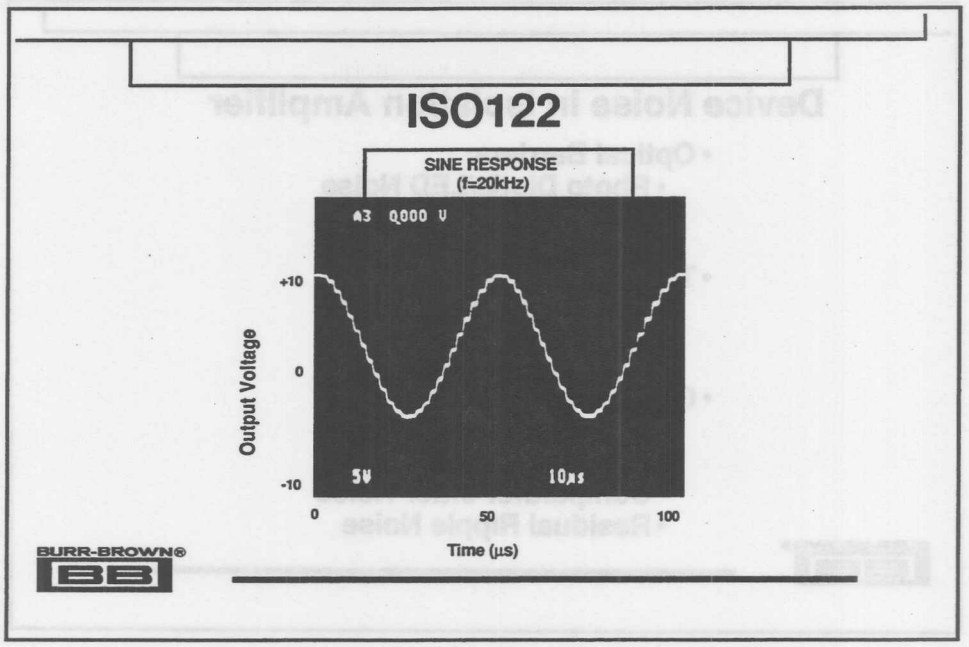
The first and most obvious type of noise is device noise. This noise is generated inside a component, such as a resistor or an op amp. The second category of noise is conducted noise. Conducted noise is present in the conductive paths of the circuit, such as the metal traces going to the input of the isolation amplifier or the power supply lines. And finally, radiated noise, also known as electromagnetic interference, enters the circuit via E-fields or B- fields, causing undesirable interference with the signal of interest.



Device Noise in Isolation Amplifier

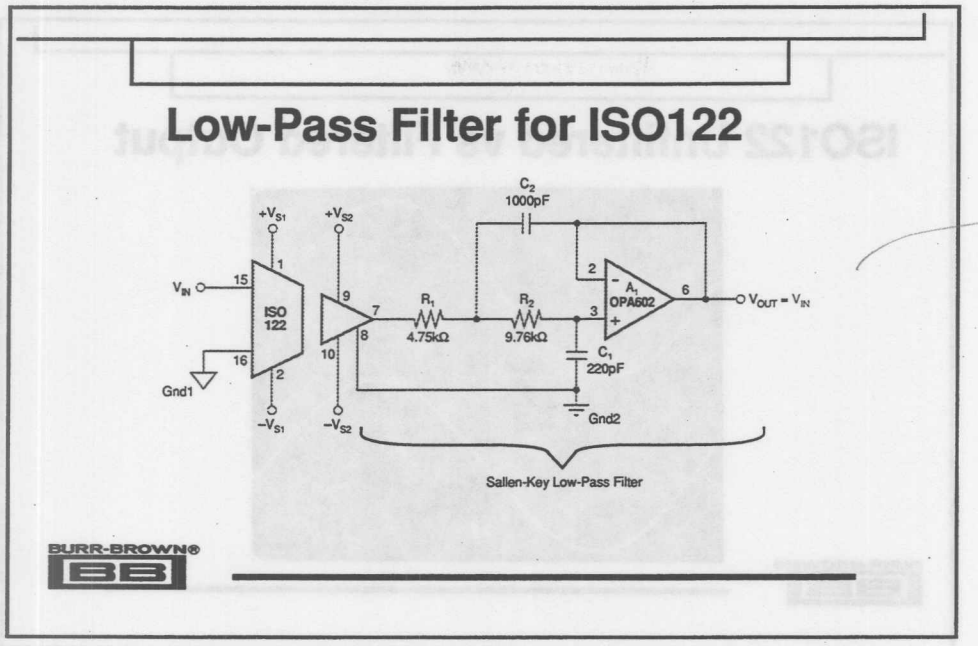
Isolation amplifiers with optical barriers have device noise that is generated primarily by the internal amplifiers and their feedback networks. The noise calculation for these amplifiers is easily equated to classical transimpedance amplifier noise calculations. This noise is most easily eliminated with filtering at the output of the device. Toriod barrier isolation amplifiers also have the internal amplifier noise as well as a residual ripple noise. This ripple noise voltage is a by-product of the modulation / demodulation design structure of the isolation amplifier. The residual ripple has a fundamental frequency component equivalent to the modulation frequency, which is above the signal bandwidth of the isolation amplifier.

The capacitive barrier isolation amplifier also requires an analog to digital modulation in the input stage of the amplifier and then a digital to analog demodulation on the output side of the isolation barrier. This process creates a residual ripple voltage on the output of the amplifier.



ISO122

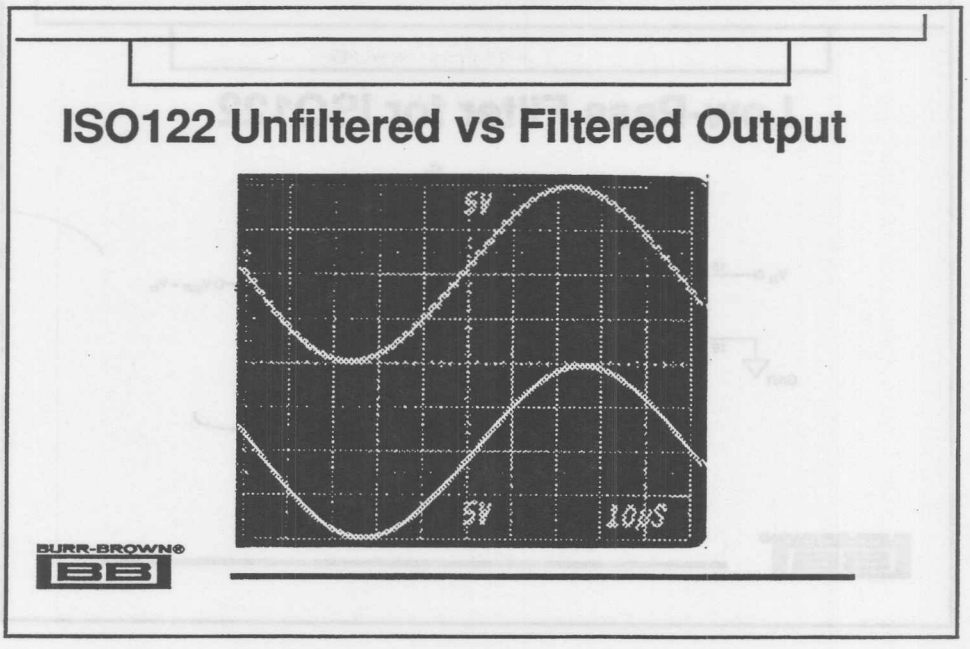
The quantization effect can be seen in this scope photo. This photo illustrates the output signal of a 20kHz signal through the ISO122. This is an illustration of the ISO122, capacitive coupled isolation amplifier. The input signal is integrated through A_1. That signal is compared to a 500kHz oscillator. The comparator output produces is duty cycle representation of the analog input which is then transmitted across the isolation barrier. The transmitted signal is sensed by the output stage of the isolation amplifier and demodulated back to an analog signal.



see APP 23 p 115

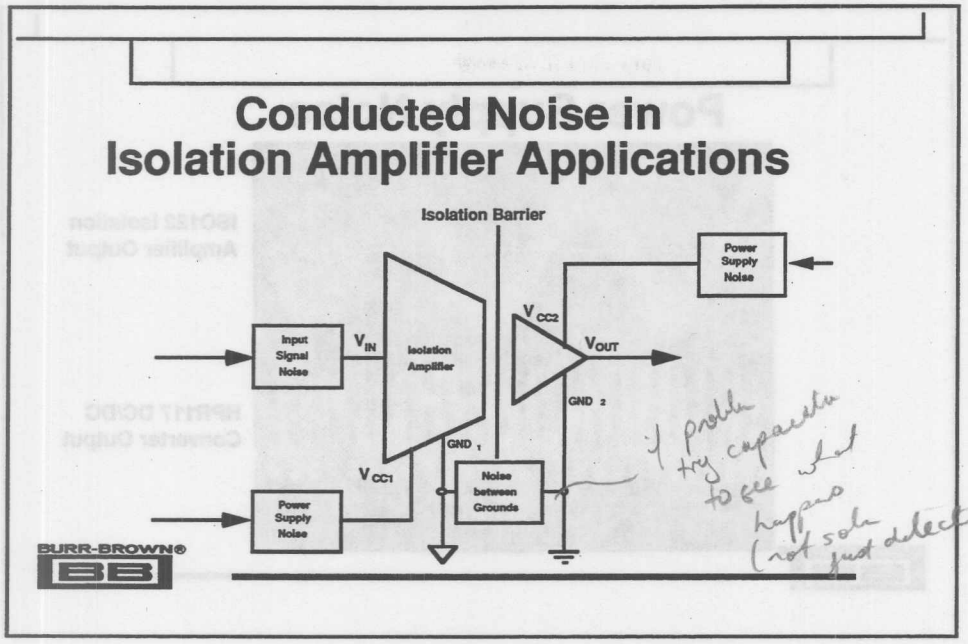
Low-Pass Filter for ISO122

A Sallen-Key, low-pass filter on the output of the ISO122 eliminates the 500kHz ripple voltage without compromising the 50kHz bandwidth of the amplifier. The filter shown here is a 50kHz, two- pole filter with a Q equal to 1. Overall, this filter produces a three-pole Butterworth response and eliminates the output ripple. This filter is easily designed using the FilterPro design kit provided by Burr-Brown.



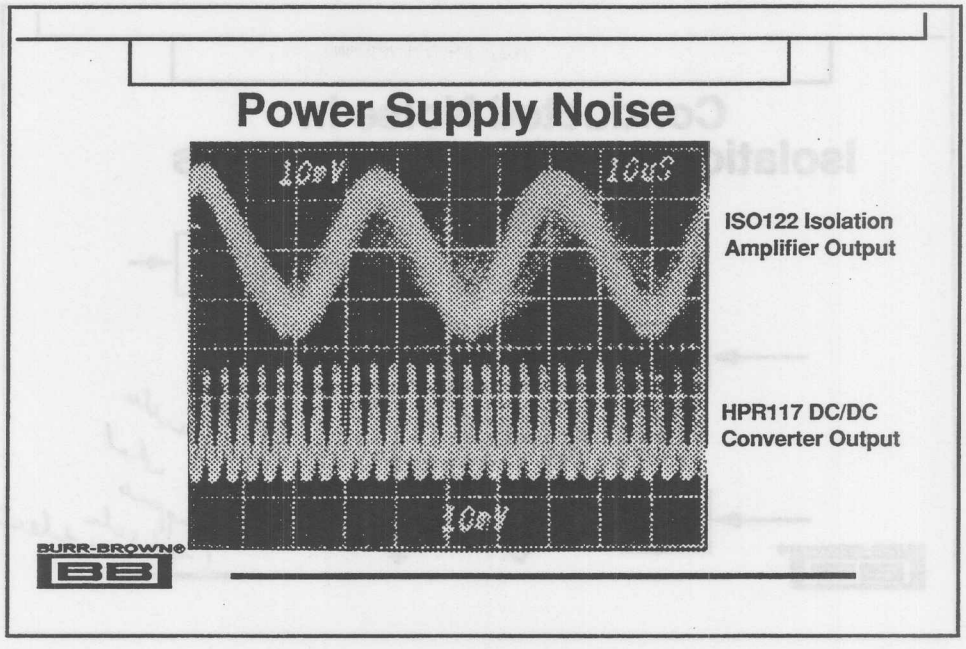
ISO122 Unfiltered vs Filtered Output

The top trace of the scope photo is the output of the ISO122 without the Butterworth filter. The bottom trace shows how the ripple is removed by the filter.



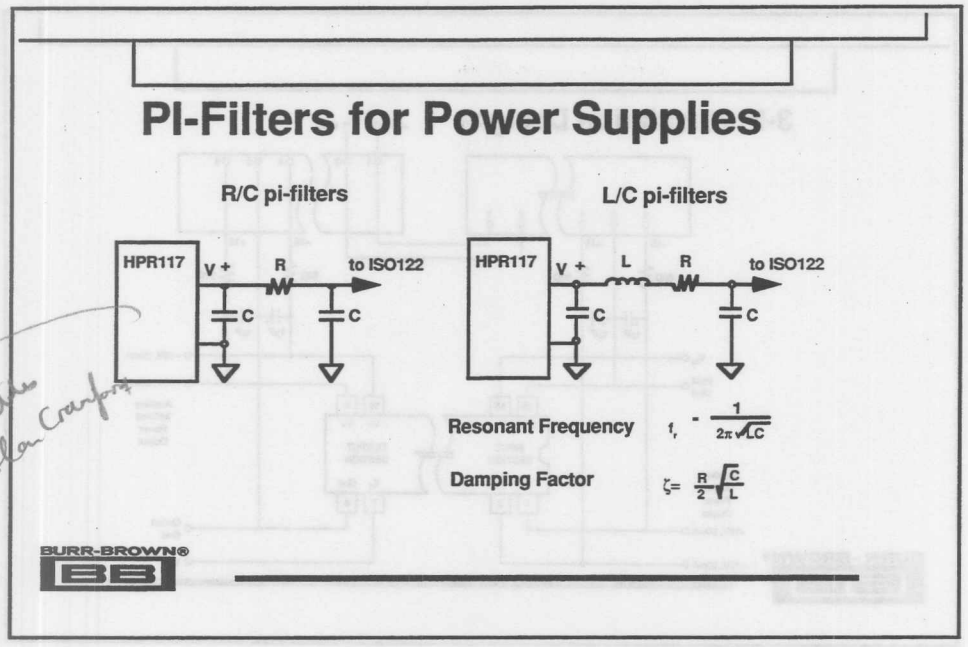
Conducted Noise in Isolation Amplifier Applications

The second source of noise, conducted noise, can be coupled into the signal path through the input of the amplifier, between the grounds and through the power supply trace. Low frequency noise at the input of the isolation amplifier is difficult to eliminate without compromising the bandwidth performance of the circuit. High frequency noise at the input of the isolation amplifier may or may not be filtered by the isolation amplifier. The optical coupled isolation amplifiers are able to reject high frequency input noise because of the inherent low noise transmission of the signal across the barrier. In contrast, the toriod and capacitive coupled amplifiers use a modulation frequency to transmit the signal across the barrier. The modulation frequency can interact with the high frequency noise and alias a small error signal into the bandwidth of the amplifier. It is a good rule of thumb to use a filter before the input of these isolation amplifiers to eliminate high frequency noise from the system.



Power Supply Noise

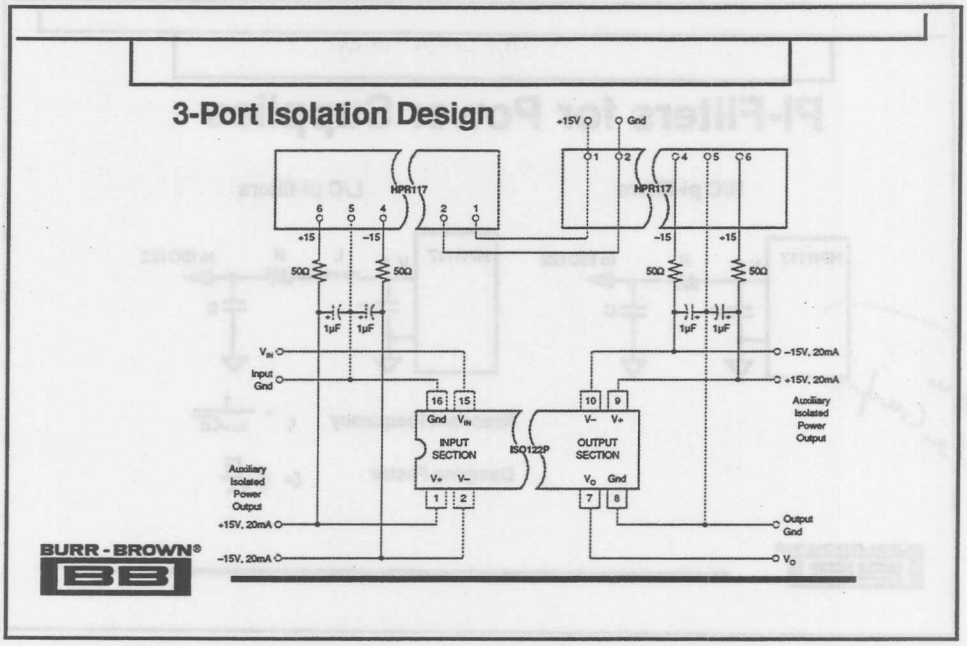
Power supply ripple can also interact with the modulation/demodulation frequency to alias noise into the isolation amplifier's bandwidth. In this photo, the top trace is the ISO122 output noise due to the aliasing effect of the power supply ripple. The bottom trace illustrates the power supply ripple of the HPR117 DC/DC converter. The error that has been generated at the output of the ISO122 due to the interaction with the HPR117 supply ripple is a 30kHz, 30mV_{p-p} noise.



PI-Filters for Power Supplies

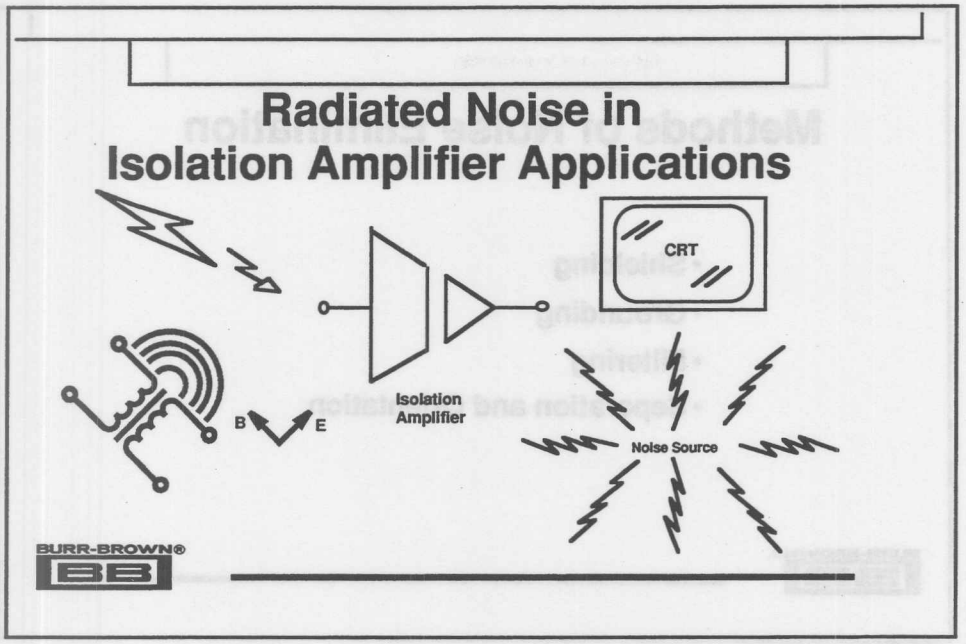
Proper by-pass capacitors is not enough. A pi-filter is needed to eliminate this interaction. Both pi-filters act as a low-pass filters. The R/C filter is easier to design, however, the voltage drop across the resistor effects the regulation of the power supply. The L/C filter eliminates that problem by using an inductor instead of a resistor in the power line path. This circuit is prone to gain peaking and a small value resistor is used to damp the effects.

AB 24
P117



3-Port Isolation Design

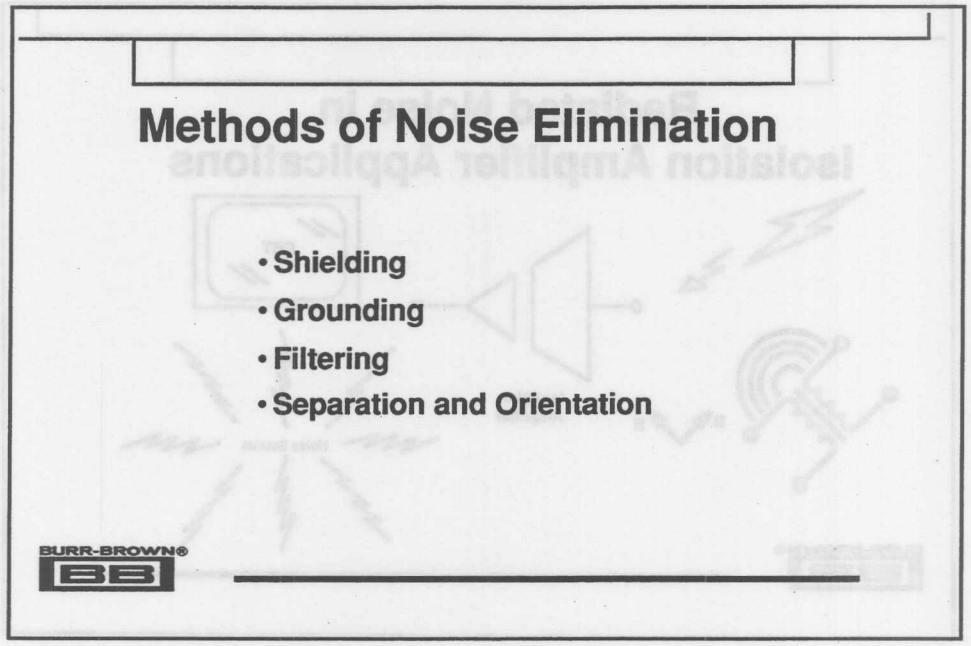
In the case of the ISO122/HPR117 problem an R/C filter is designed. Here the output capacitance of the HPR117 is used for one of the capacitors and a 50Ω resistor is placed in the power line path. This filter eliminates the $30mV_{p-p}$ noise shown in the previous scope photo.



Radiated Noise in Isolation Amplifier Applications

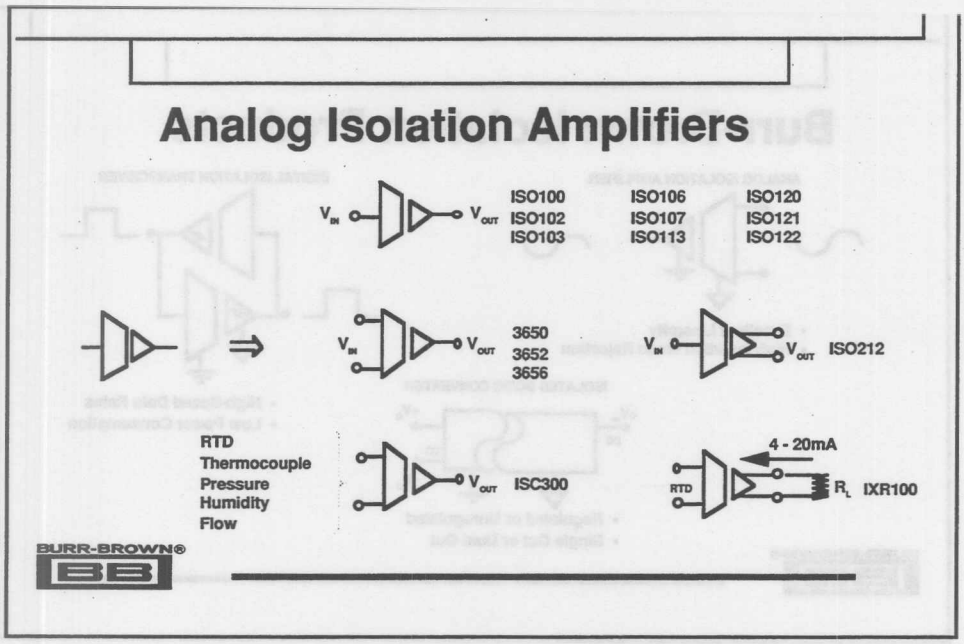
Radiated noise is transmitted through air into high impedance nodes. There are numerous sources for radiated noise such as ground plans, power planes, switching networks, inductors, toriods, etc. Some isolation technologies are more sensitive to radiated noise interference than others. For instance, the toriod isolation amplifiers are more sensitive to B-field radiation, the capacitive isolation amplifiers are more sensitive to E-field radiation. Radiated noise, also called EMI, can easily be identified as a problem by experimenting with the proximity of a circuit to a radiating device or by experimenting with shielding techniques.

INSTEAD of μ METAL → copper or conductive tape



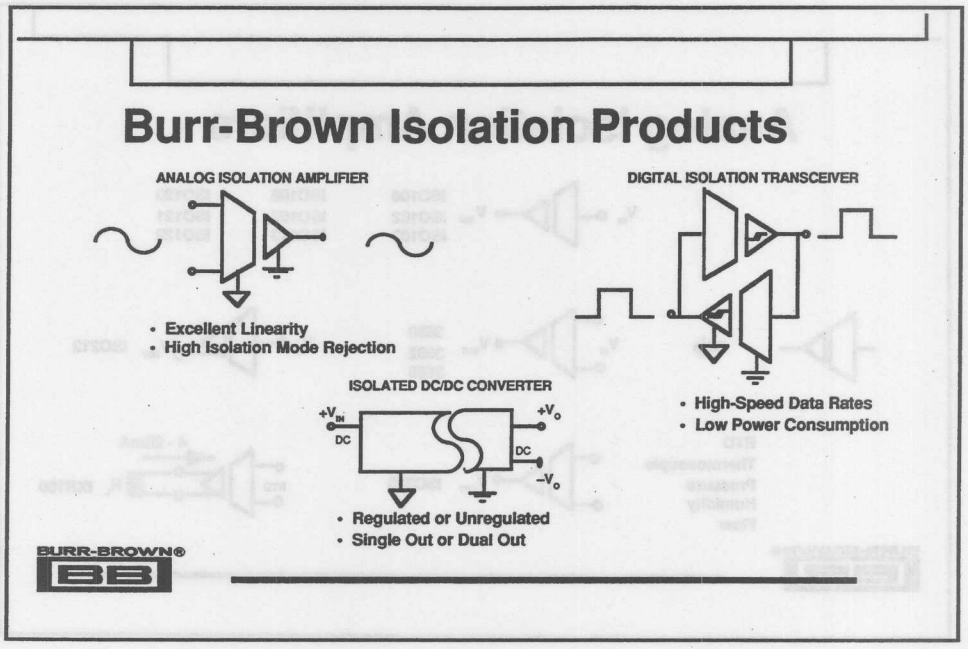
Methods of Noise Elimination

Once radiated noise is identified as the problem several methods of elimination can be used. Shielding materials should be selected to match the type of radiation, be it a B-field or E-field effect. Separation from the radiating source or orientation to the problem field lines is another effective technique to eliminate interference problems.



Analog Isolation Amplifiers

Isolation amplifiers are available in several input/output configurations. The voltage input options available are single ended, differential ended and senor ready. The output options range from single ended to differential. Some isolation amplifiers are available with power on the chip, others require external power.



Burr-Brown Isolation Products

Isolation amplifiers, DC/DC converters, and digital couplers act as an interface between remote sensors, motors, and data acquisition systems, where low signal levels are detected and amplified. In the presence of high voltages, these devices provide galvanic isolation between the input and output potentials so to prevent personnel or equipment damage. This concludes the section on isolation applications and solutions. Are there any questions?

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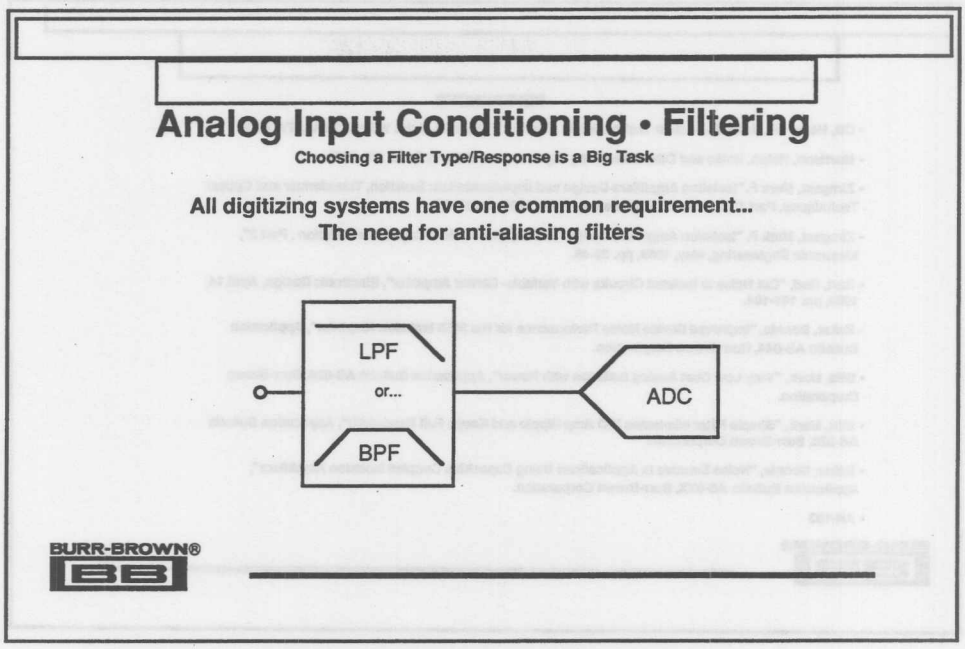
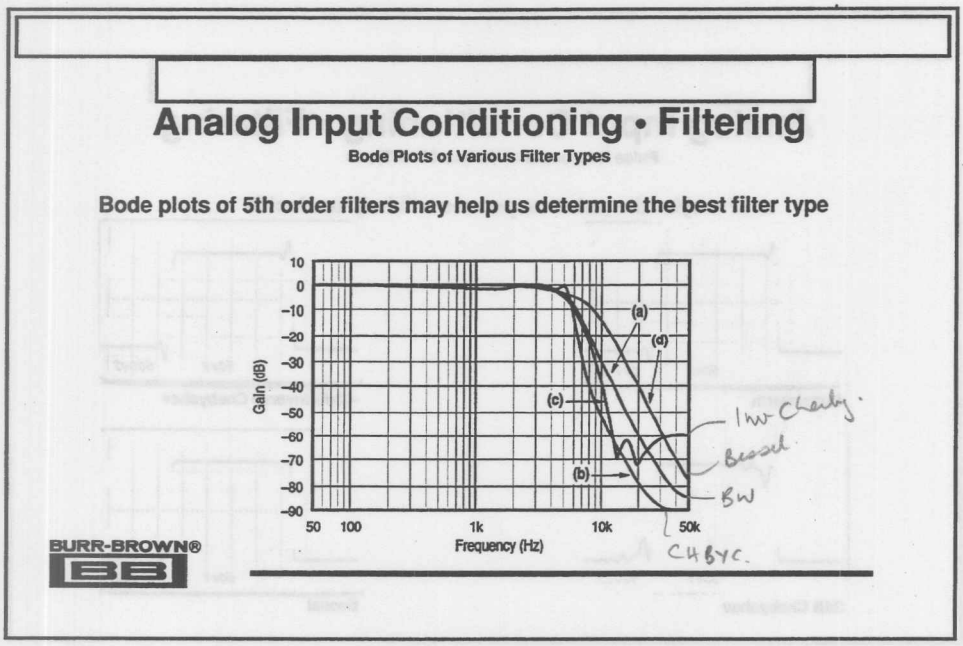


Analog Input Conditioning • Filtering

Choosing a Filter Type/Response is a Big Task

Now that we know that all digitizing systems must be preceded by an anti-aliasing filter, the task is to determine how to implement it. Only a low pass filter is required for anti-aliasing purposes, however, for your particular application you may desire a band pass response to remove lower frequencies. For instance, a DC component could be removed with a band pass filter before additional gain is applied to a small ac component. There are several filter types including the tuned circuit, Butterworth, Chebyshev, Inverse Chebyshev, and Bessel from which to choose, and you might want either a low pass or band pass response. The types each have their own advantages, and these are covered in more detail in Burr-Brown Application Bulletin #35 (AB-035) "Filter Design Program For The UAF42 Universal Active Filter". However, if you are going to do any complex digital signal processing, the task of type selection just got easier. You will probably opt for the Bessel due to its linear phase characteristics and the pulse response.



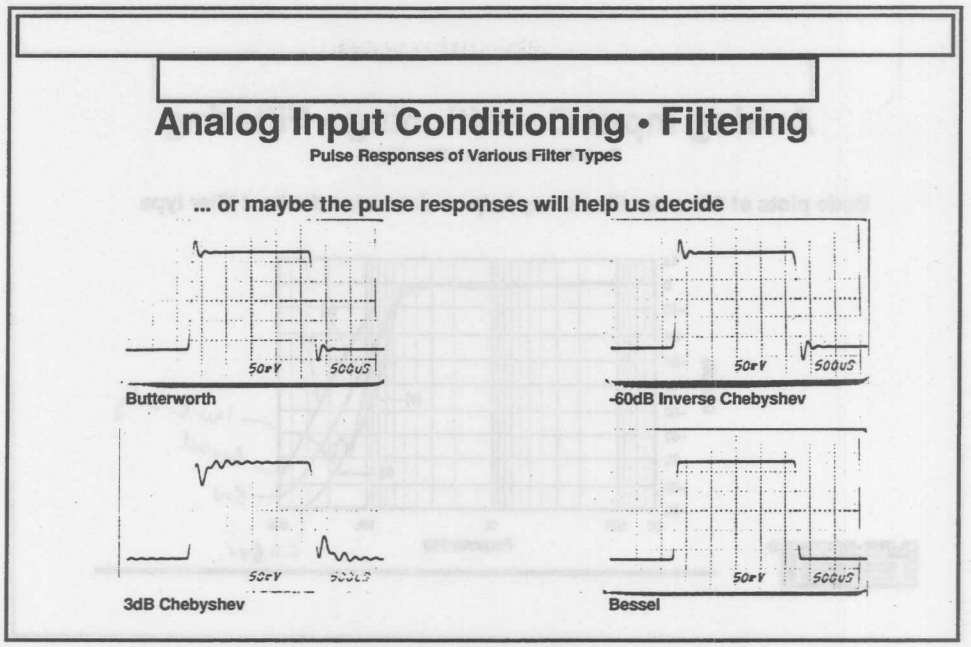
Analog Input Conditioning • Filtering

Bode Plots of Various Filter Types

If you're not doing DSP, the task of selection continues. Shown here are bode plots for various filter type implementations of 5kHz low pass filters. (a) Butterworth • shows its flat pass band response (the most flat of all types discussed here) and fairly steep rate of attenuation in the transition band. (b) Chebyshev • shows the pass band ripple but extremely steep rate of attenuation in the transition band. (c) Inverse Chebyshev • shows the ripple in the stop band at a lower level of attenuation while maintaining fairly flat pass band gain and attenuation rate. (d) Bessel • characterized by its fairly flat pass band gain and slow initial rate of attenuation.

→best for step functions

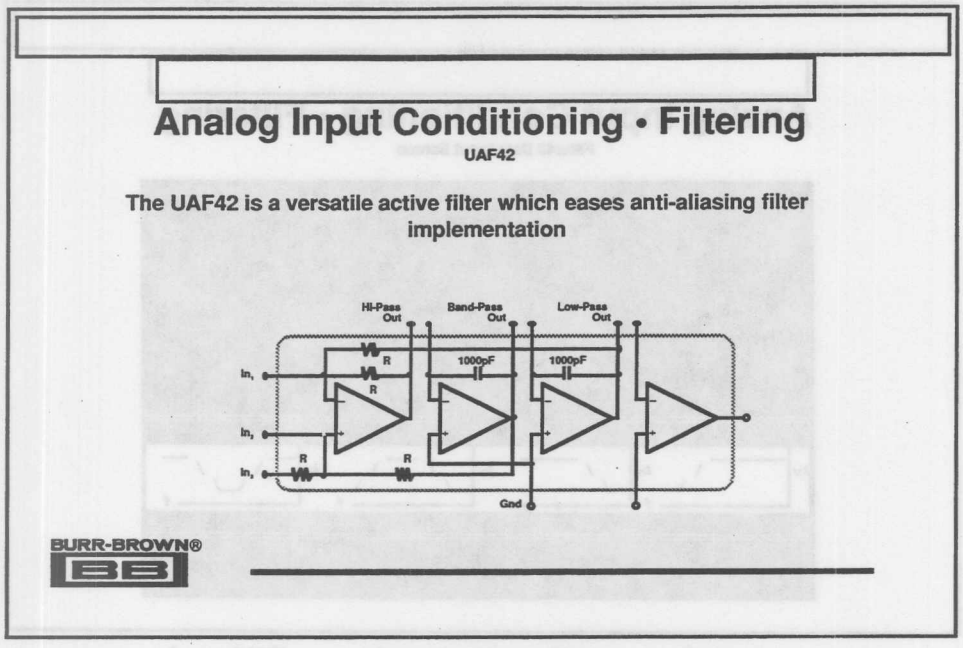
slew rat $= 2\pi f E$?



Analog Input Conditioning • Filtering

Pulse Responses of Various Filter Types

As stated earlier, the Bessel exhibits the best pulse response of the types discussed. The ringing in the Chebyshev make it useless in most step or impulse applications, while the moderate overshoot and ringing of the Butterworth and Inverse Chebyshev may be acceptable.

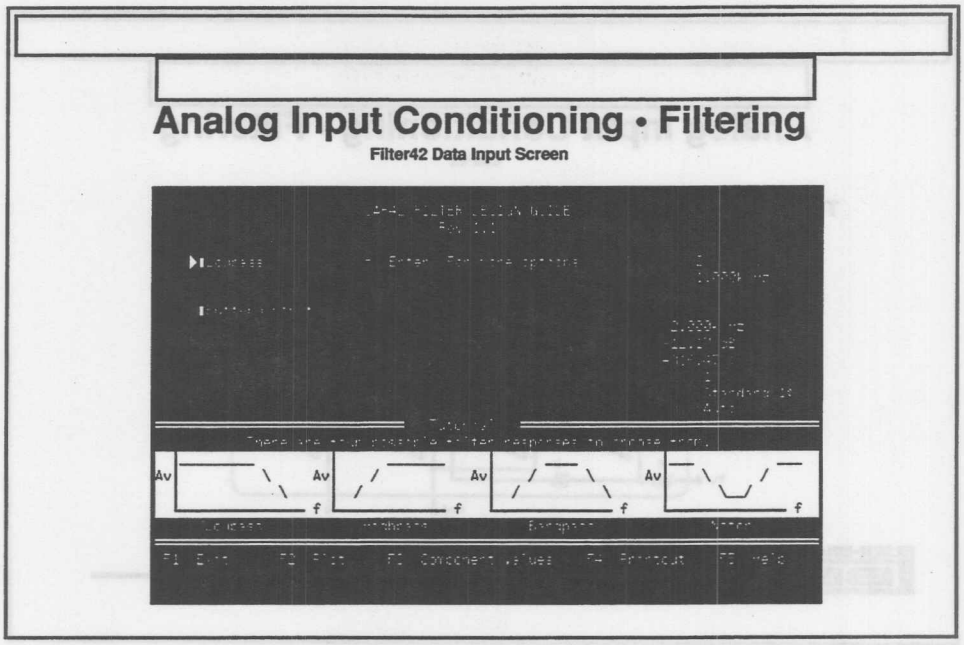


Analog Input Conditioning • Filtering

UAF42

If your upper frequency of interest is less than about 100kHz, then the UAF42 provides an easy way to get up to three poles (in the form of one pole pair and one real pole). Many second order filters can be realized with the UAF42 and just two resistors. The internal caps are trimmed to 0.5% - try that with discrete caps at an affordable price. Multiple UAF42s can be cascaded for filters of the umpteenth order, really aiding you when you take your design from paper to PC board.

The UAF42 provides a completely time continuous filter which is free of switching noise (which may be aliased), and the state-variable topology provides low sensitivity of filter parameters to external component values. For two pole designs, the A4 amplifier can be used as in input or output buffer.

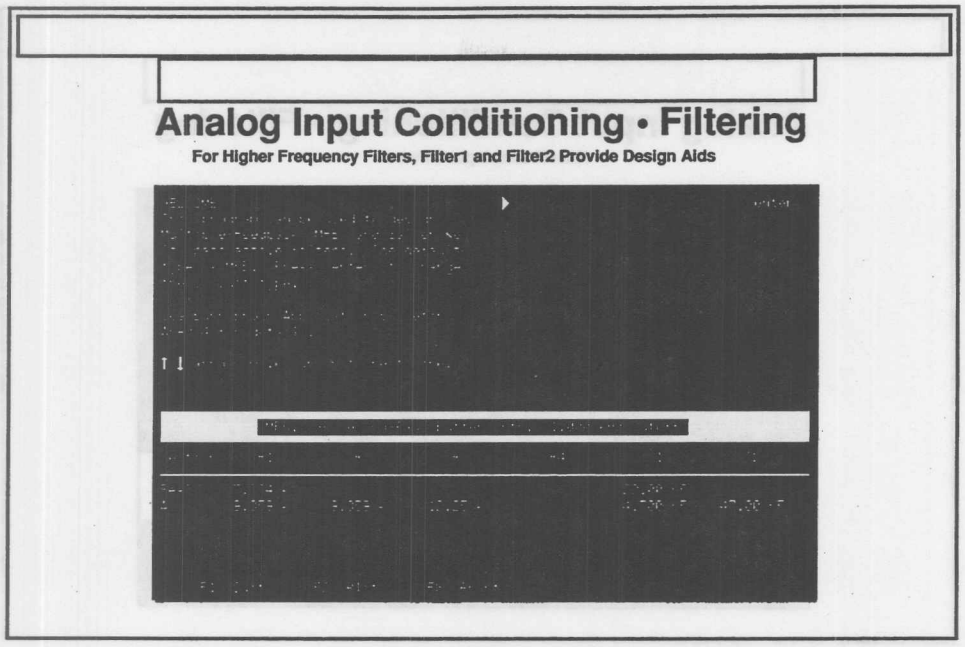


Analog Input Conditioning • Filtering

Filter42 Data Input Screen

Filter design with Filter42, the UAF42, and Burr-Brown's Application Bulletin #35 (AB-035) takes what used to be a very tedious task and simplifies it beyond belief. Just enter the filter response, type, order (Q for band pass) and corner frequency ...voila, the filter is instantly designed (well, maybe a second for an 8088 based PC). The data entry screen will also calculate and display magnitude and phase for a given frequency entered into the filter response area. A block diagram with subsections corresponding to schematics in the Filter42 documentation simplify schematic capture or circuit assembly, and a bode plot showing magnitude and phase response is also available on EGA or higher resolution monitors. Filter42's bode plot can be used to display a stored response in addition to the current design for easy comparison of filter designs. The bode plot can be printed by using your PC's operating system for screen dumps (drivers for HP Laser printers and other are included with the disk).

AB 035



Analog Input Conditioning • Filtering

For Higher Frequency Filters, Filter1 and Filter2 Provide Design Aids

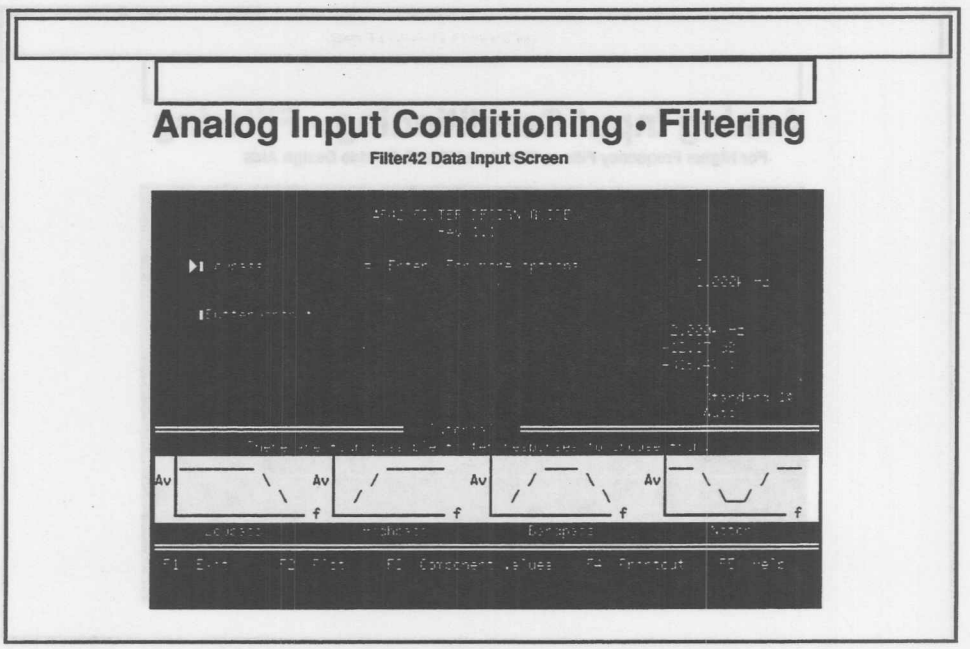
Sallen Key.

All op amps eventually turn into low pass filters due to the op amp's open loop gain curve. In general, the unity gain bandwidth (UGBW) of an op amp should be at least fifty times the amplifiers gain (non-inverting) times the filter's corner frequency, and there is also error due to the open loop gain of the op amp.

$UGBW > 50 \bullet Gain \bullet f_o$

$$\%_{error} = 100 \bullet \left(\frac{1}{\sqrt{1 + f_o^{\,2} + Gain^2 / UGBW^2}} \right)$$

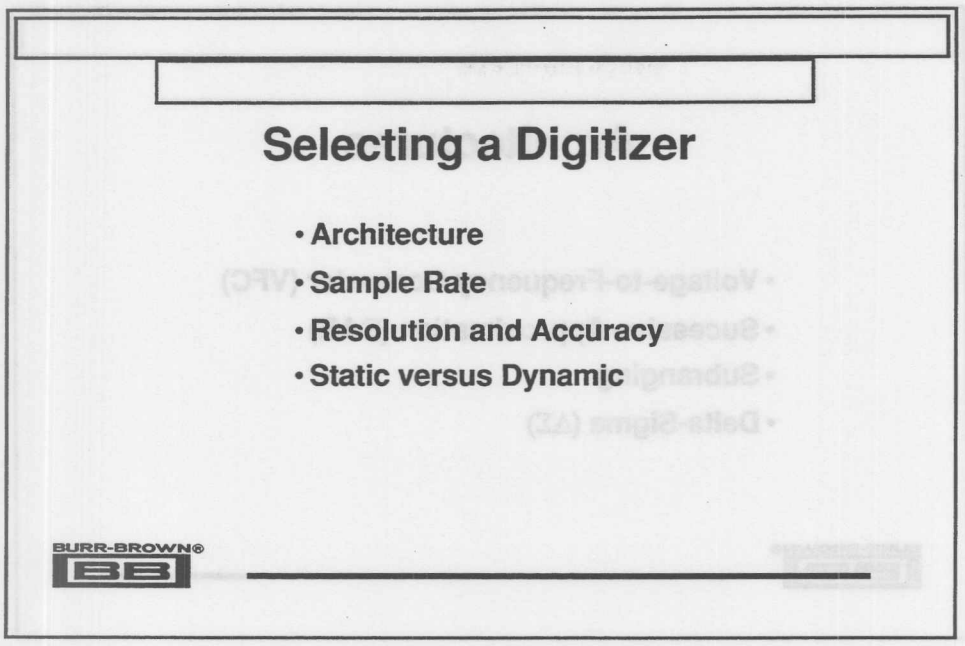
Therefore, for higher frequency filters you need faster op amps - kinda makes sense doesn't it. For designing other filters, Burr-Brown provides two other filter design utilities: (1) Filter1 (Burr-Brown Application Bulletin #17) • "Sallen-Key Low-Pass Filter Design Program", (2) Filter2 (Burr-Brown Application Bulletin #34) • "MFB (Multiple Feedback) Low-Pass Filter Design Program". Using these utilities you can choose your own op amps to best suit your application . All three utilities (these two and Filter42) are available on the FilterPro diskette, and should be accompanied with AB-017, AB-034, and AB-035 hard copy documentation.



Analog Input Conditioning • Filtering

Filter42 Data Input Screen

Filter design with Filter42, the UAF42, and Burr-Brown's Application Bulletin #35 (AB-035) takes what used to be a very tedious task and simplifies it beyond belief. Just enter the filter response, type, order (Q for band pass) and corner frequency ...voila, the filter is instantly designed (well, maybe a second for an 8088 based PC). The data entry screen will also calculate and display magnitude and phase for a given frequency entered into the filter response area. A block diagram with subsections corresponding to schematics in the Filter42 documentation simplify schematic capture or circuit assembly, and a bode plot showing magnitude and phase response is also available on EGA or higher resolution monitors. Filter42's bode plot can be used to display a stored response in addition to the current design for easy comparison of filter designs. The bode plot can be printed by using your PC's operating system for screen dumps (drivers for HP Laser printers and other are included with the disk).



Selecting a Digitizer

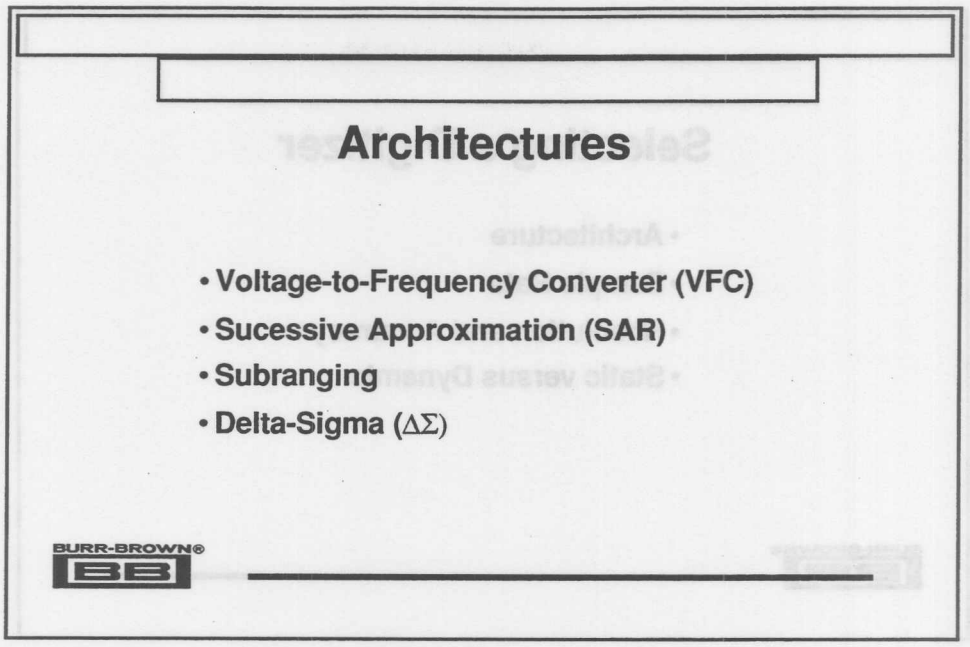
When selecting the right digitizer for your application, there are four main elements to consider:

1. System requirements will often dictate which ADC architectures are acceptable.

2. Sampling rate of the ADC can be determined by the frequency of the analog input signal and the data update rate requirements.

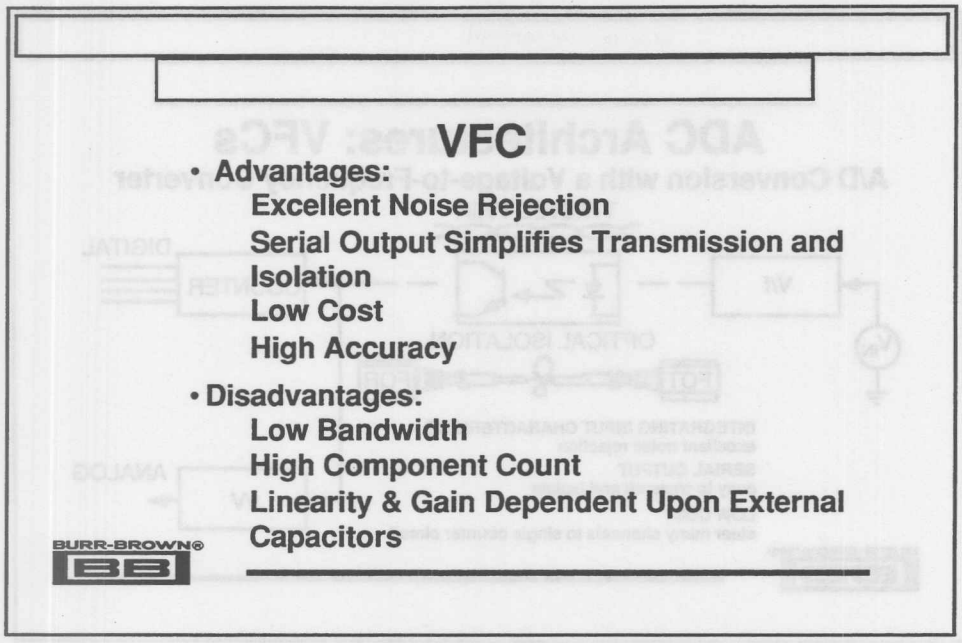
3. Resolution and accuracy can be determined by examining the properties of the input signal, as well as the overall system accuracy needs.

4. Static systems, such as motion control, temperature and pressure measurement, pattern recognition and others require good DC accuracy. Dynamic systems, such as wave form digitization, digital audio and communications generally require good AC characteristics while absolute accuracy may not be important.



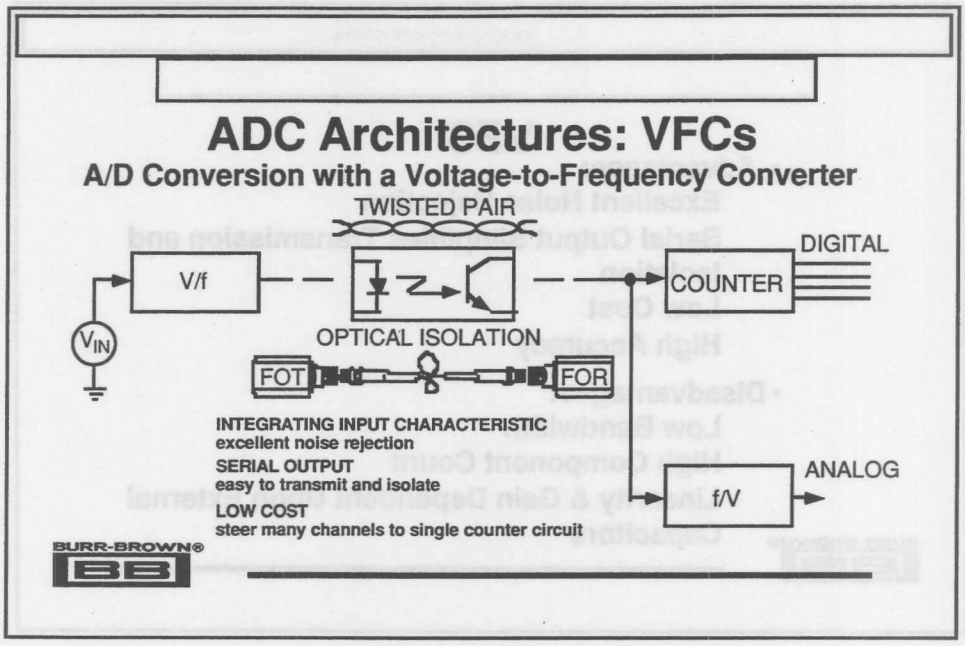
Architectures

For this seminar, we will consider four architectures and the associated advantages and disadvantages, as well as methods to improve the performance and cost reduce these architectures.



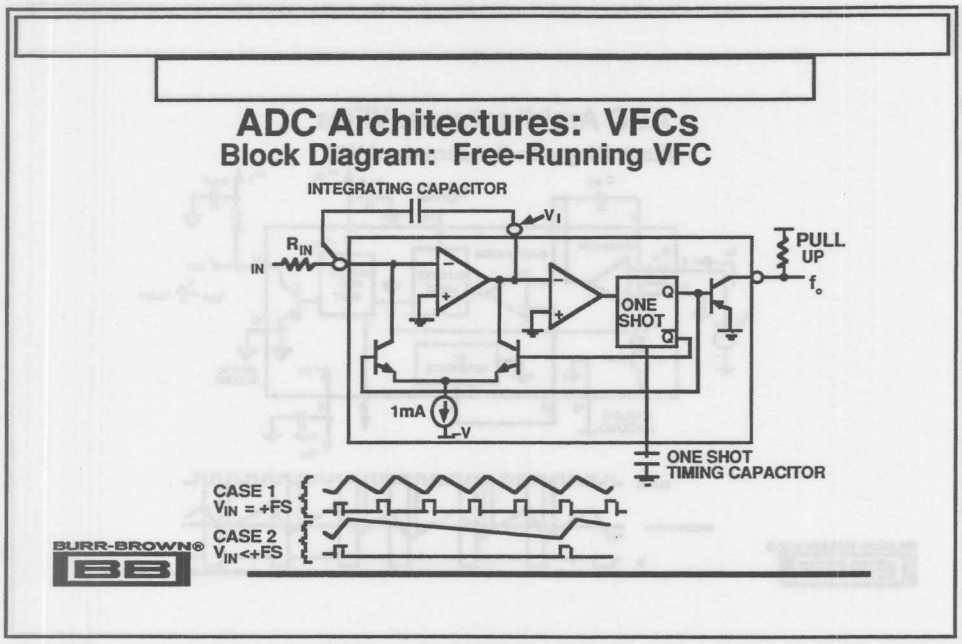
VFC

The first architecture we will examine is the Voltage-to-Frequency converter. The main advantages of this approach include noise reduction, ease of isolation and very high accuracy at a relatively low cost. The key disadvantage is limited bandwidth, as well as reliance on external components.



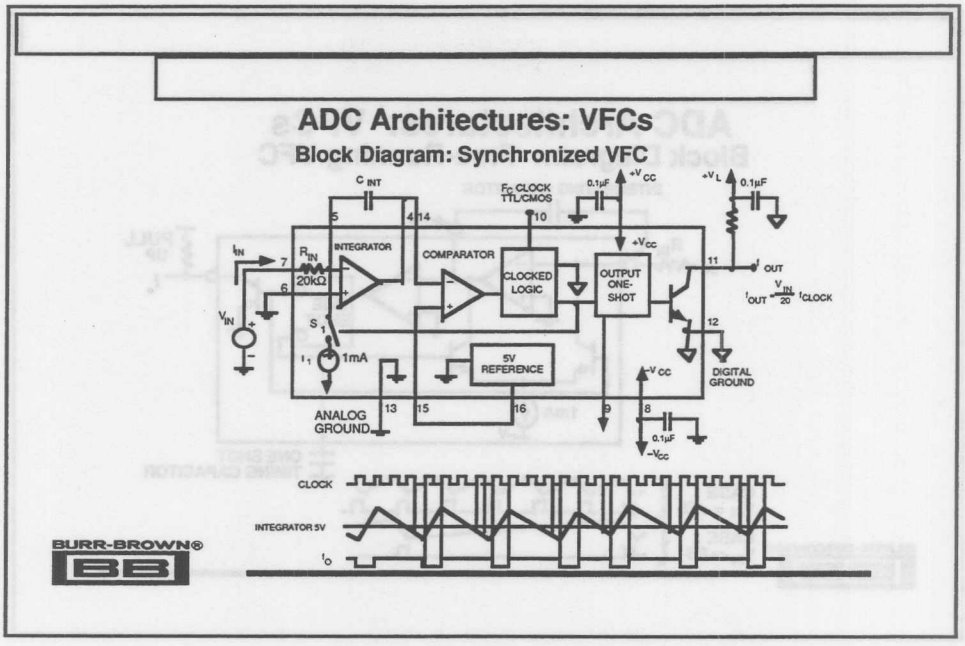
ADC Architectures: VFCs

A voltage-to-frequency converter may be used as an ADC by using it with a counter. The VFC has the benefit of having an integrating characteristic, which allows for excellent noise rejection. In addition, the frequency output is a serial stream, making it easy to isolate, as shown here. Before discussing the ADC application of a VFC in detail, we'll look at the operation of a VFC in a bit more detail.



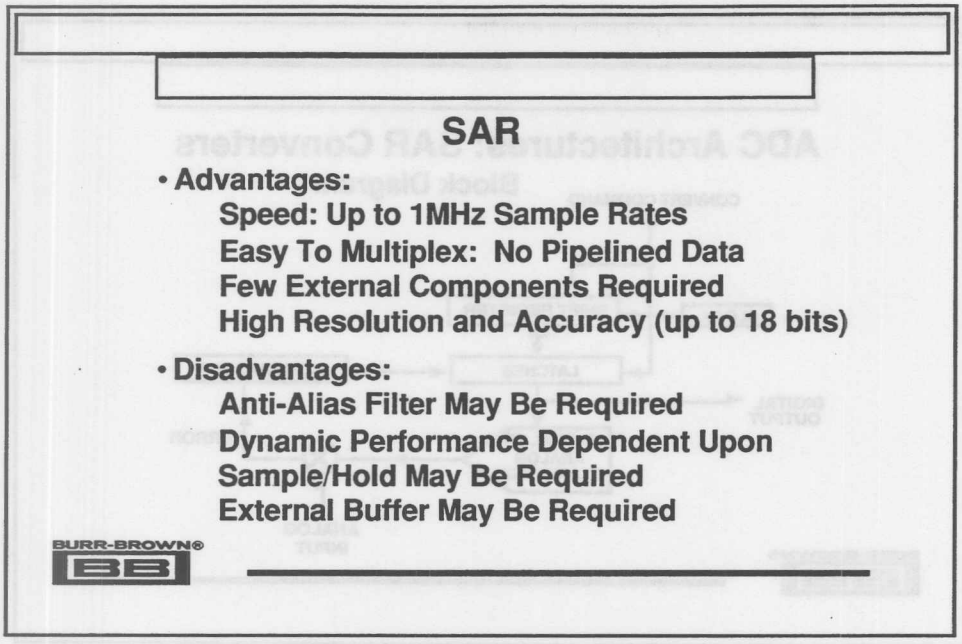
ADC Architectures: VFCs

A charge-balancing VFC is shown here. The converter integrates an analog input voltage by storing a charge in the integrating capacitor. When sufficient charge accumulates, the comparator trips, the charge drains from the capacitor during the reset period, and the one-shot generates an output pulse. Using a digital counter to tally the successive pulses moves the integration process from the analog to the digital domain. Although the frequency output of a VFC is usually measured by counting its output for a fixed period of time, if the counter is never reset, the resulting measurement is an infinite or continuous integration. This integration reduces the VFC's susceptibility to noise. While this technique is not particularly "fast", the unique capabilities of a VFC make it a viable choice for some A/D conversion requirements.



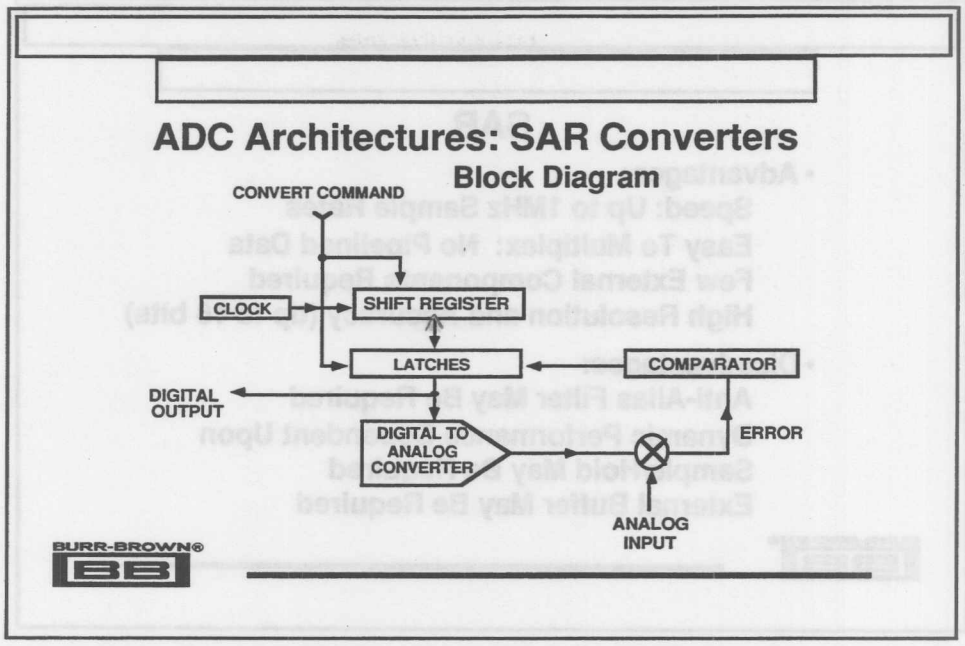
ADC Architectures: VFCs

Synchronized VFCs, such as the VFC100 shown here, simplify the counting circuitry by making the frequency output a synchronized submultiple of the system clock. This also eliminates the need for a one-shot and its associated timing capacitor.



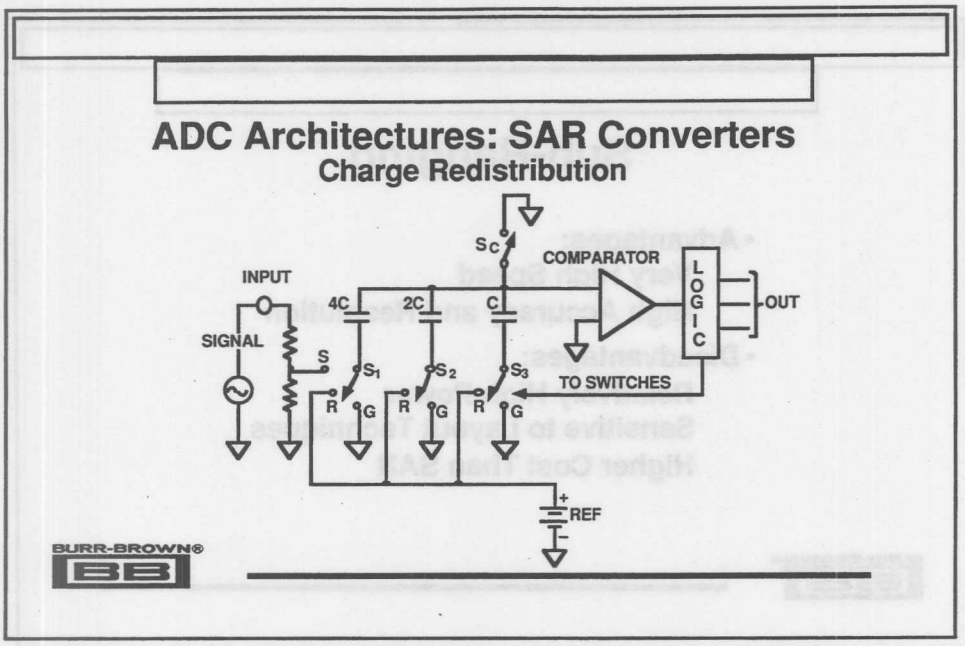
SAR

Next, we'll examine the one of the most popular architectures, Successive Approximation. SAR converters have acheived this popularity because there is an excellent cost/performance ratio. These converters address a wide variety of applications from a standpoint of speed and accuracy. They are generally easy to use and require few external components. The list of disadvantages are shrinking as technology advances, as we'll examine later.



ADC Architectures: SAR Converters

This is a block diagram of a practical successive approximation ADC. The logic-controlled current source is a digital-to-analog converter (DAC). The shift register is used to shift the convert command pulse to different bit weights, so that the successive approximation process may occur. The latch stores the information from the comparator, and after a given number of clock cycles, the process is complete to the number of bits that the converter latch is designed for.

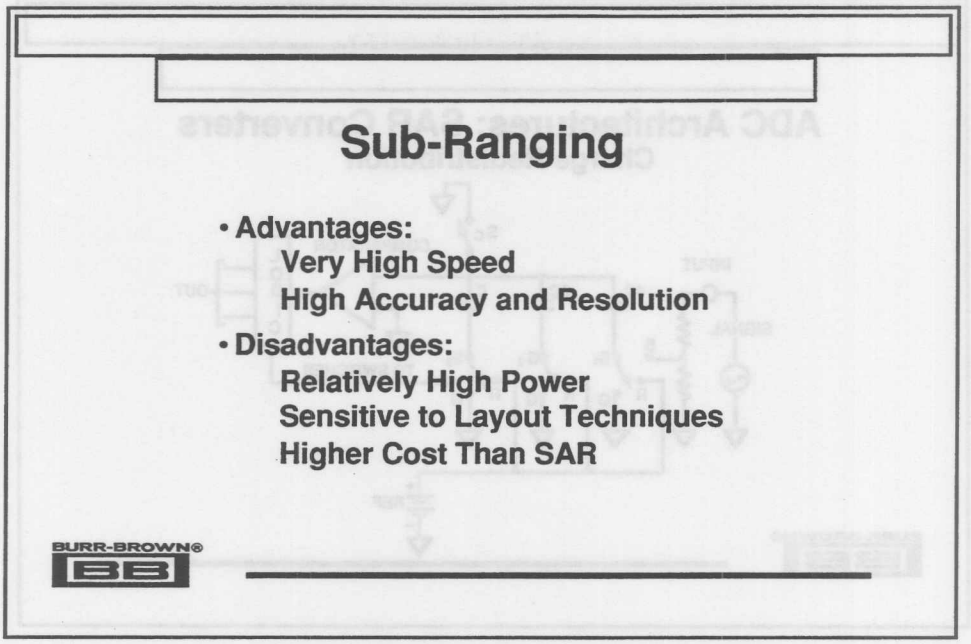


ADC Architectures: SAR Converters

Some CMOS successive approximation converters today use a charge-redistribution scheme for the DAC, instead of a conventional R-2R ladder. This example shows a 3-bit charge-redistribution ADC. This C-DAC based approach, used in converters such as our ADS7800, has the added benefit of bringing the sampling mechanism inside the ADC package. While in the sampling mode, the capacitor array switch for the MSB (S1) is in position "S", so that the charge on the MSB capacitor is proportional to the voltage level of the analog input signal, and the remaining array switches (S2 and S3) are set to position "R" to provide accurate bipolar offset from the reference source REF. At the same time, switch SC is also in the closed position to auto-zero any offset errors in the CMOS comparator.

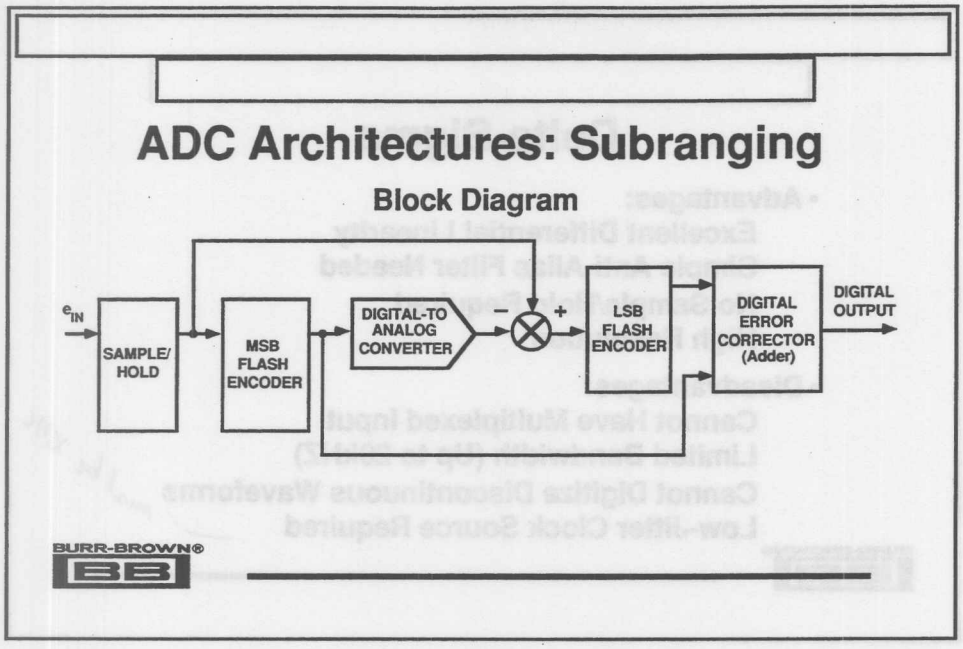
When a convert command is received, switch SC is opened to trap a charge on the MSB capacitor proportional to the input level at the time of the sampling command. Similarly, a charge is trapped on the rest of the array capacitors proportional to the reference voltage REF. The total charge trapped on the capacitor array (representing the input signal and offset) can now be moved between the three capacitors in the array by connecting switches S1, S2, and S3 to position "R" (to connect to REF) or "G" (to connect to GND) successively, changing the voltage seen at the comparator input node.

The first approximation connects the MSB capacitor via switch S1 to REF, while switches S2 and S3 are connected to GND. Depending upon whether the comparator output is HIGH or LOW, the logic will then latch S1 in position "R" or "G", and moves on to make the next approximation by connecting S2 to REF and S3 to GND. When the three successive approximation steps are made for this simple converter, the voltage level at the comparator will be within 1/2 LSB of GND, and the data output word will be based on reading the positions of S1, S2, and S3.



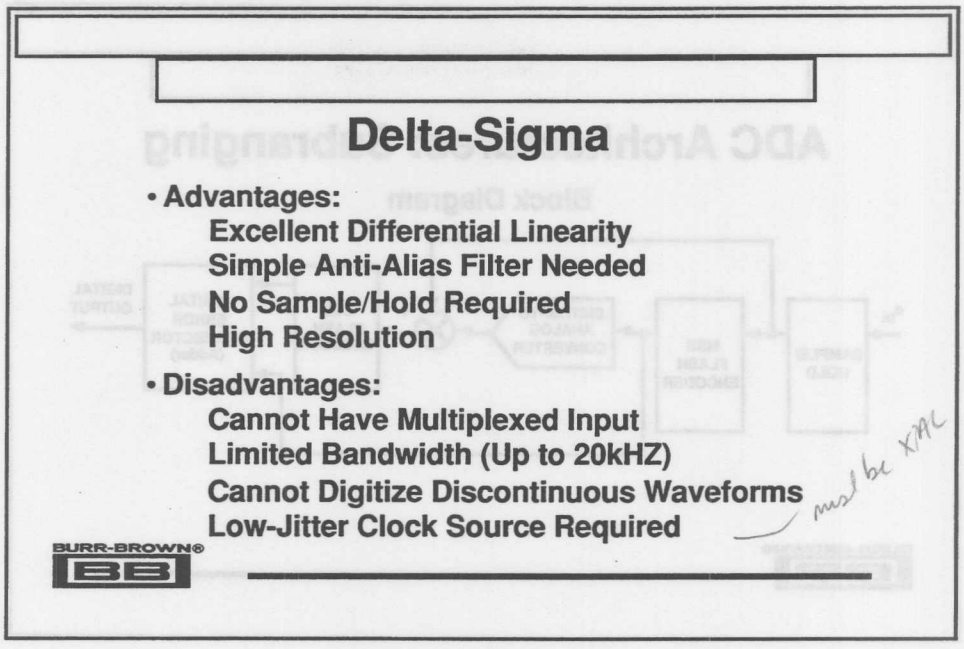
Sub-Ranging

The next architecture to look at is sub-ranging. These ADCs typically are needed when a combination of very high speed and high resolution are required. When resolutions of 12 bits or greater are required at conversion rates above 1MHz, sub-ranging ADCs are an ideal choice. And, like the SAR converters discussed previously, technology advances are reducing the list of disadvantages.



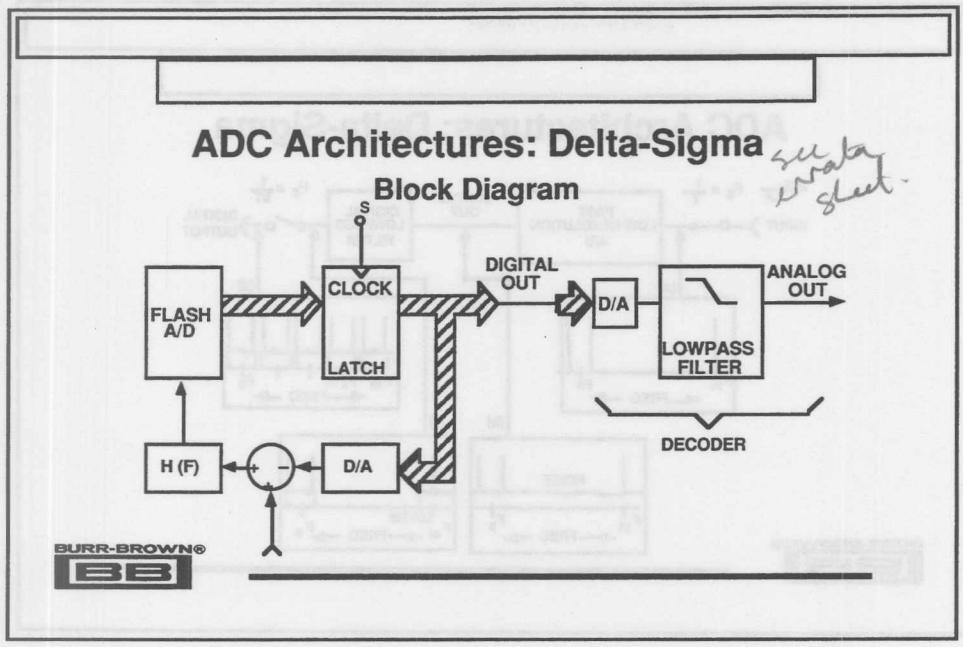
ADC Architectures: Subranging

A subranging ADC uses two or more low-resolution ADCs and digital error correction to achieve high resolution. In this block diagram, taken from our 12-bit ADC603, the input signal is sampled by a sample/hold amplifier, then converted by a 7-bit flash converter. These 7 bits are then reconstructed through a very accurate 7-bit DAC. Thus, an analog version of the 7 MSBs of the converted signal is provided to the subtraction circuit, which subtracts this reconstructed signal from the original input signal. The resulting residue (error) output is amplified and then converted by another 7-bit LSB flash converter, and these 7 bits are then combined with the 7 MSB bits in the digital correction circuitry to provide a highly linear 12-bit output. Note that a two bit overlap is used to provide the error correction.



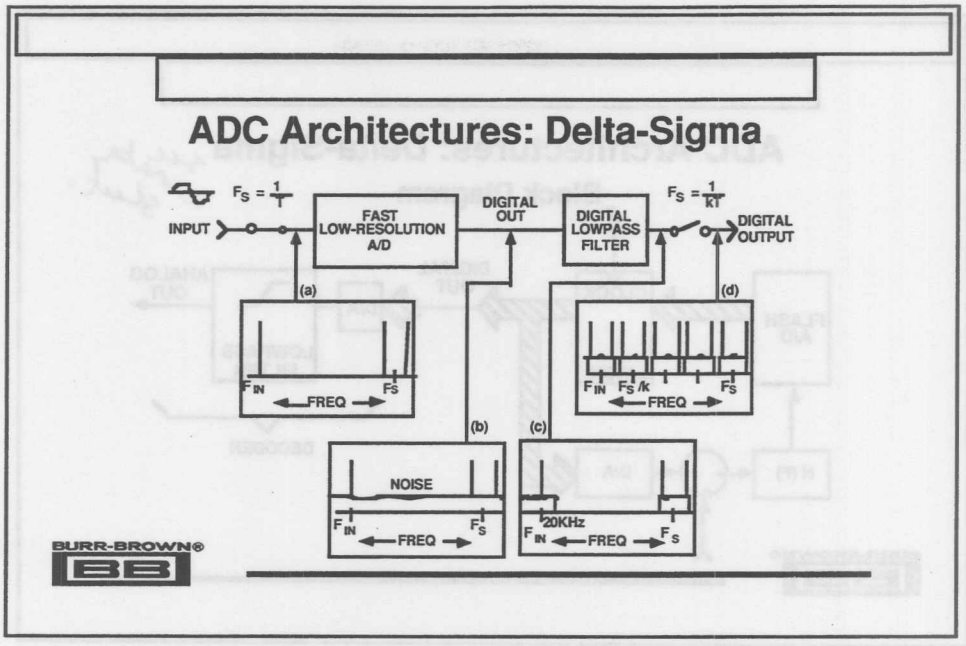
Delta-Sigma

The final architecture we'll look at is Delta-Sigma, which is one of the newest and most talked about approaches. The main reason for the high level of interest in using this approach is the high oversampling rate, which reduces or eliminates the need for anti-aliasing filters. Key disadvantages to Delta-Sigma converters include limited bandwidth and the inability to digitize discontinuous wave forms.



ADC Architectures: Delta-Sigma

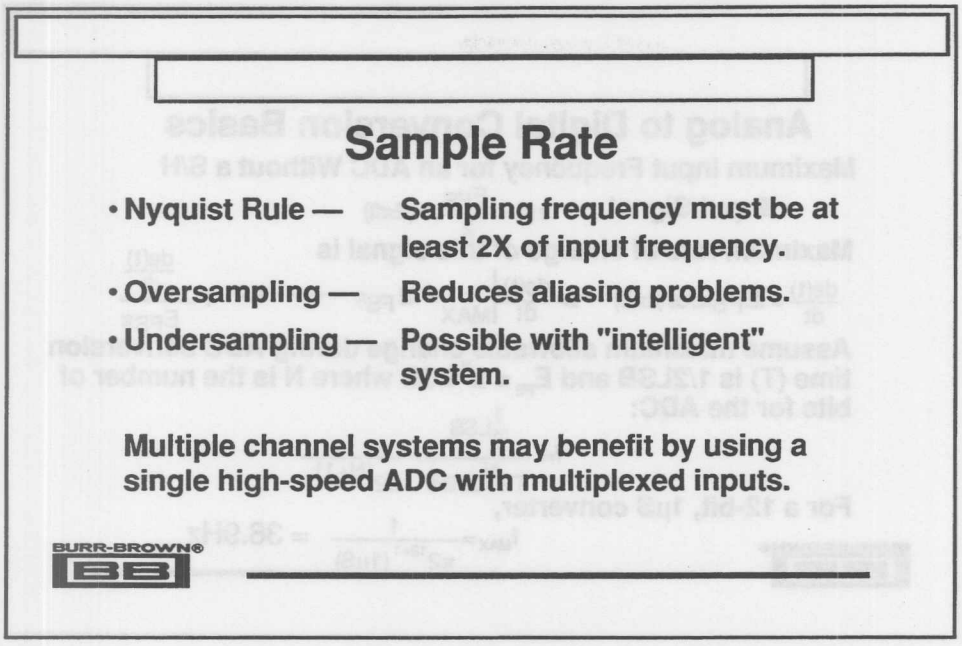
This diagrams shows the architecture of a typical "noise-shaping" delta-sigma converter. The input signal is converted by a low resolution flash ADC, and that digital word is reconstructed into analog, then subtracted from the input signal. The residue, or error, signal is filtered and then converted again. This process repeats several times, until the integrated error becomes negligible. Meanwhile, all of the resulting digital outputs are sent to a digital filter to create a higher-resolution output. The transfer function of the analog filter used (H(f)) can be made to "shape" the quantization noise so that it is minimized in the eventual signal passband (after the digital filter), but at a cost of increasing it outside the passband, where it will presumably do little harm.



ADC Architectures: Delta-Sigma

The first notable characteristic of a delta-sigma converter is that it is a highly OVERSAMPLING converter. The block diagram here shows the operation of such a converter, and the noise response of the converter at different points in the conversion process. These converters take considerable advantage of the reduction in quantization noise by oversampling, as discussed previously.

Delta-sigma converters are attractive because they require no sample-hold and because they are produced on a digital process (i.e. no laser trimming is required).



Sample Rate

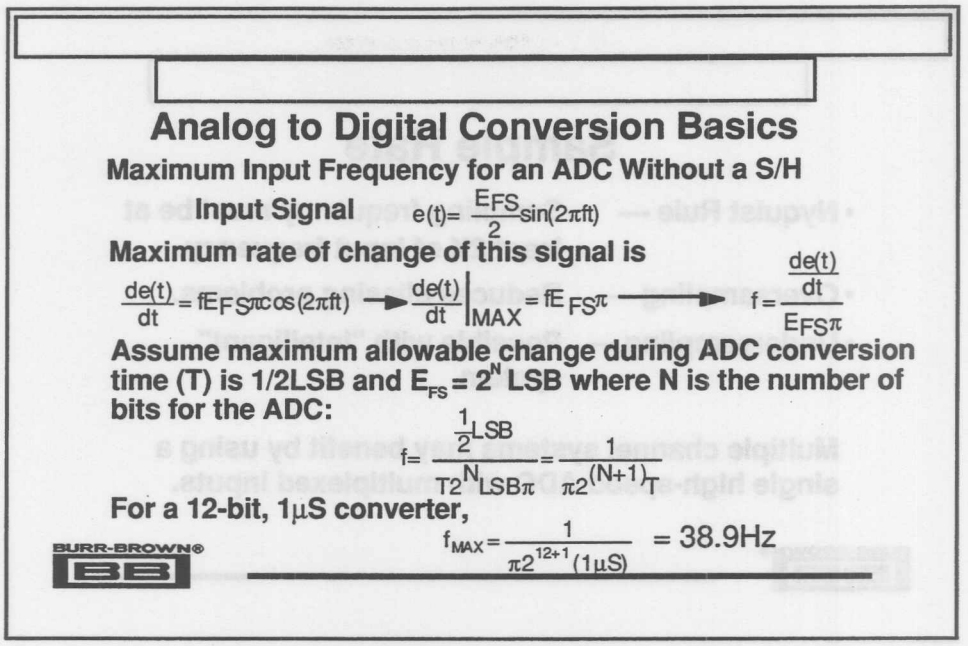
Now that we have discussed differences in various architectures, let's look at a few of the key requirements which can help you to choose the correct architecture.

The first element is sample rate. Two main considerations for sample rate are the frequency of the input signal which will be digitized, and how fast you need to update the digital output.

Nyquist sampling theory is an excellent rule of thumb, but deviations from the rule are possible which can both extend and enhance performance. In oversampling, the design of the anti-alias filter preceding the ADC can be simplified. This is due to the filter passband being extended. Another advantage of oversampling is improved SNR. As sampling frequency is increased with respect to input frequency, the quantization noise is spread over a wider bandwidth which reduces the RMS noise in the analog bandwidth. The expression of full-scale SNR for oversampling conditions is given by:

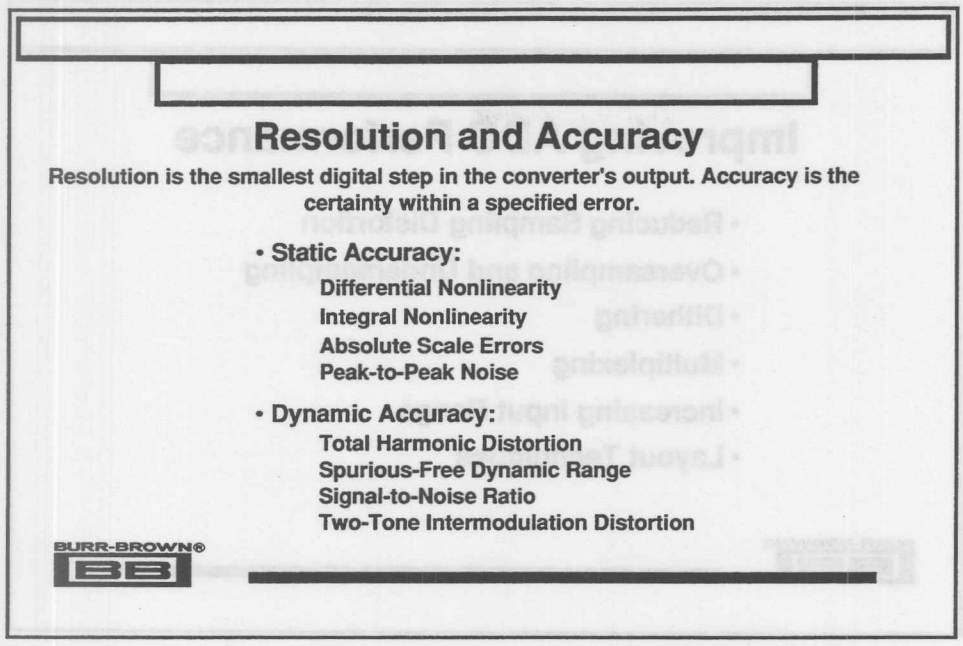
$$SNR = 6.02N + 1.76dB + 10\log_{10}(f_s/2f_a)$$

For a given input bandwidth, doubling the sampling frequency can increase SNR by 3dB, and increase effective bits by 1/2 bit.



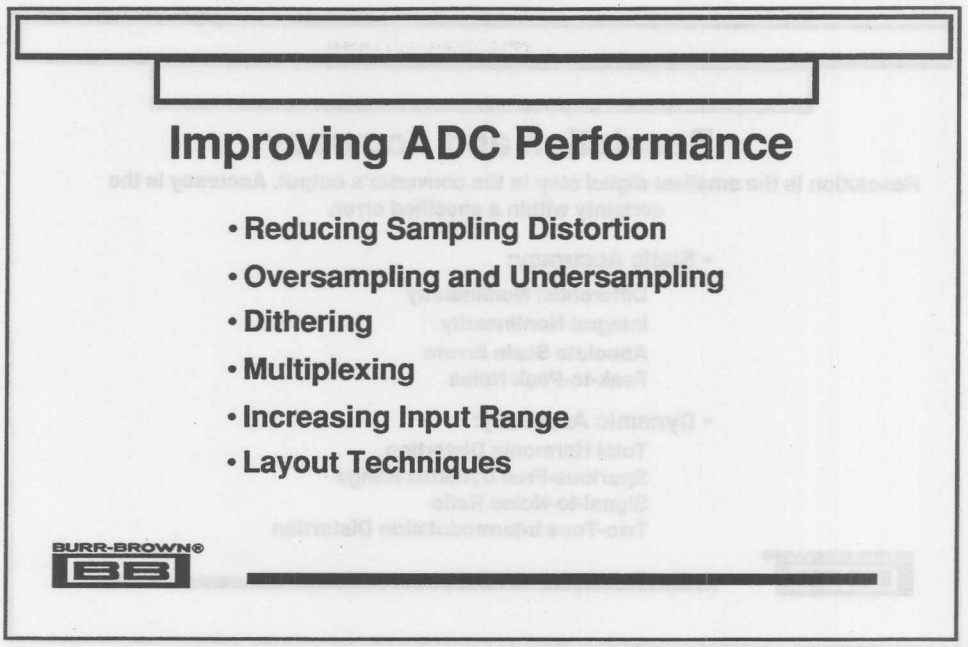
Analog to Digital Conversion Basics

You may be asking yourself at this point, "If the quantizer can change the analog voltage values into digital signals, why do you need the sampling mechanism? The answer to this question is shown in this slide. In order to achieve a specified accuracy, the signal cannot change by more than 1/2 LSB in the time ita takes for the quantizer to convert the analog voltage into its digital representation. As you can see, a very fast 12-bit quantizer (μS) would only be able to accurately digitize a full scale signal<40Hz! This is obbiously not a very practical situation. By placing a sample/hold amplifier in front of the quantizer, the signal the quantizer sees is always constant during its conversion time, and the bandwidth of the signal you can digitize now is limited by the conversion speed of the quantizer. We'll look at this in a bit more depth later.) So, by using a sample/hold amplifier, we can make that 1μS quantizer digitize 500kHz signals much more effectively. Many modern A/D converters include the sample/hold function within the IC package; nonetheless, some kind of sampling circuit is present in any high-speed converter.



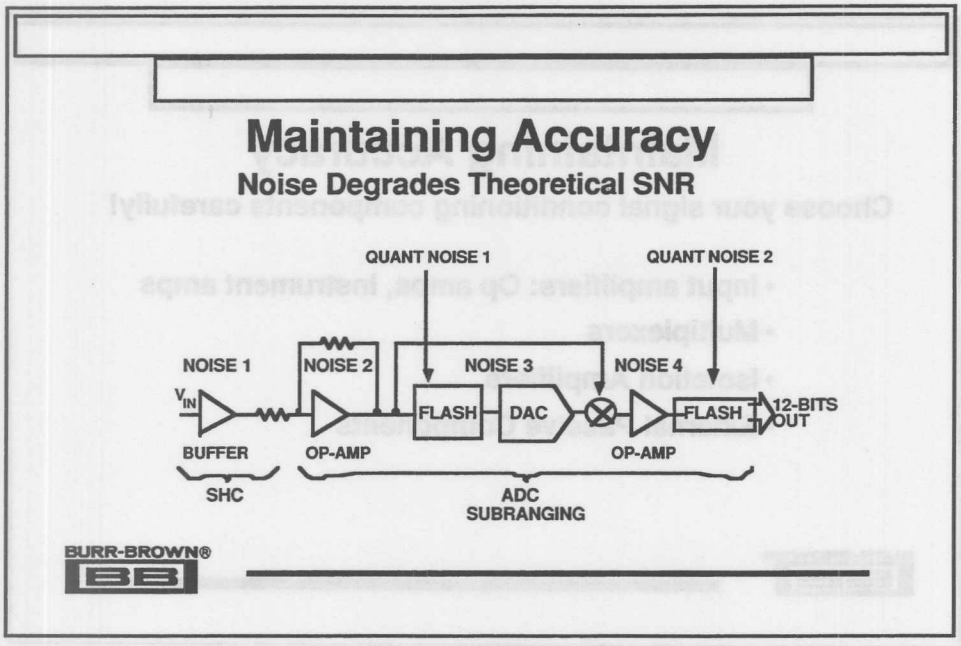
Resolution and Accuracy

It's important to note that resolution and accuracy are not the same thing in A/D converters, even though they are sometimes used interchangeably in informal conversation and advertising. Resolution relates to the smallest digital step in the converters' output. Accuracy is related to the certainty within a specified error. It's determined by the nonlinearity, offset, and gain error specifications. For example, a 16-bit ADC with 0.003% nonlinearity can move in steps of 62.5µV out of 20V full scale (1/2 LSB to16 bits), but can only be accurate to 300µV (1/2LSB to 14 bits). Beware: RESOLUTION does not imply ACCURACY nor does ACCURACY imply RESOLUTION.



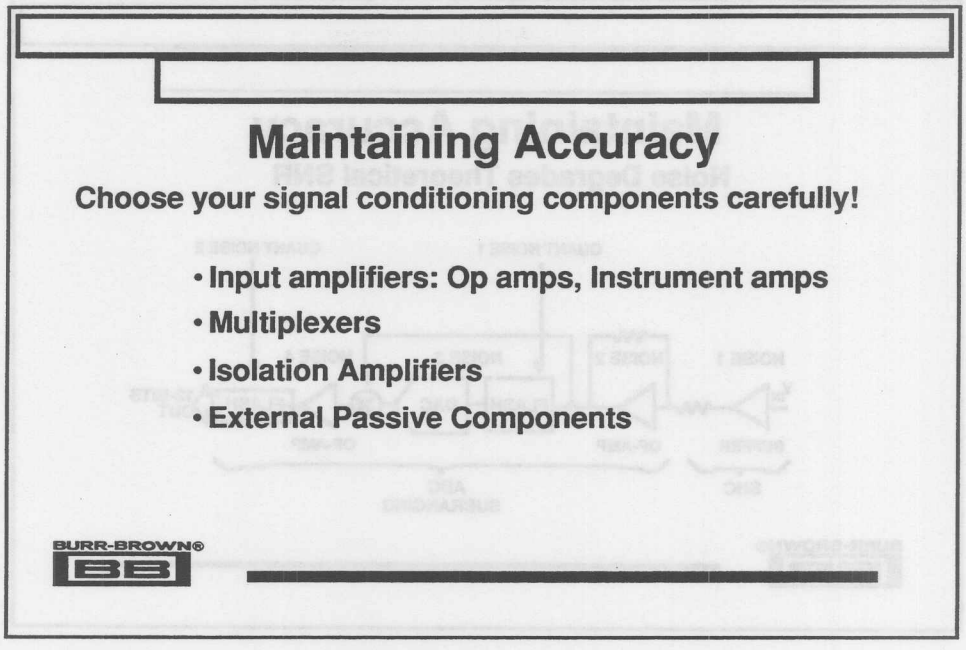
Improving ADC Performance

Next we'll look at methods to enhance performance of ADCs.



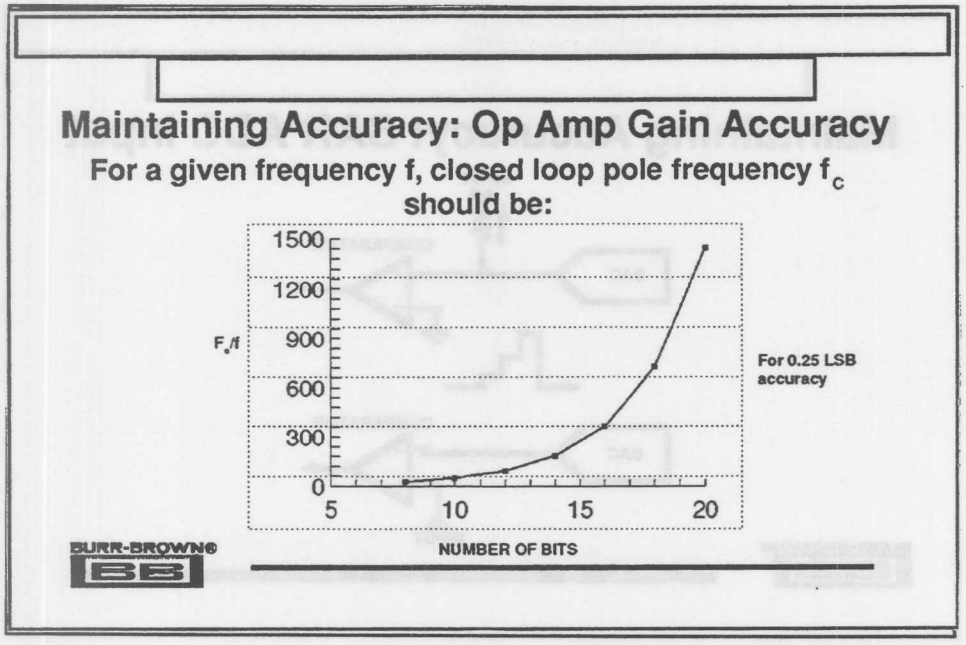
Maintaining Accuracy

In any analog-to-digital conversion system, there are several potential noise sources which can degrade the theoretical performance one might expect from the system. Amplifiers preceding the ADC have some noise associated with them, as well as the errors we looked at in the sample/hold. Of course, the quantization noise of the ADC is another consideration. In this example, the 12-bit converter should theoretically provide a SNR of 74dB - but realistically, due to the ADC's internal noise, it will only provide about 70dB of SNR.Wideband ADCs typically show the largest SNR degradation from ideal performance as the wide analog input bandwidth contains noise which is aliased into the Nyquist bandwidth.



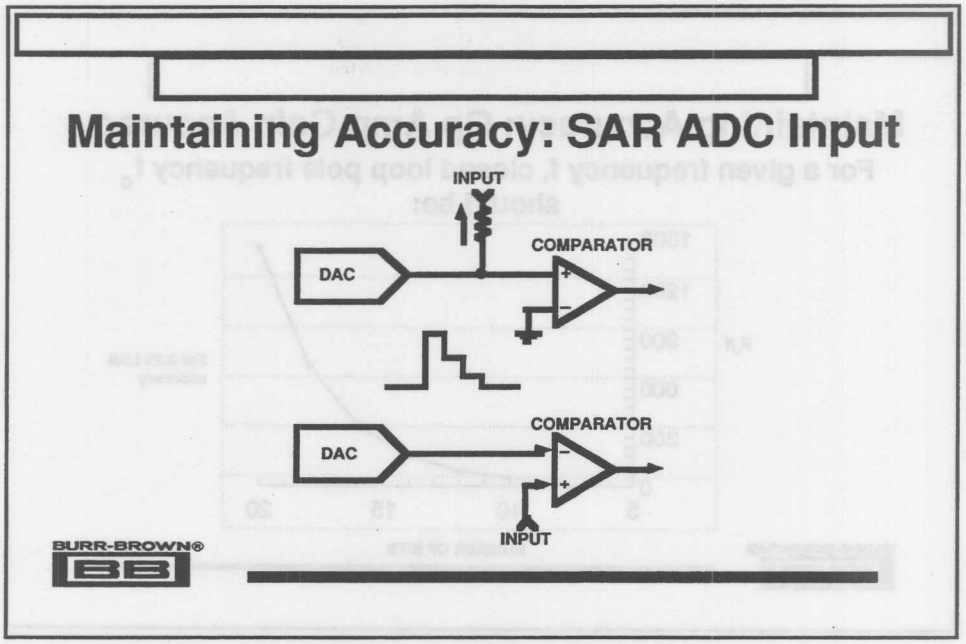
Maintaining Accuracy

We can now take a look at some considerations one must make in choosing op amps for use in circuitry preceding an A/D converter, to minimize errors and noise.



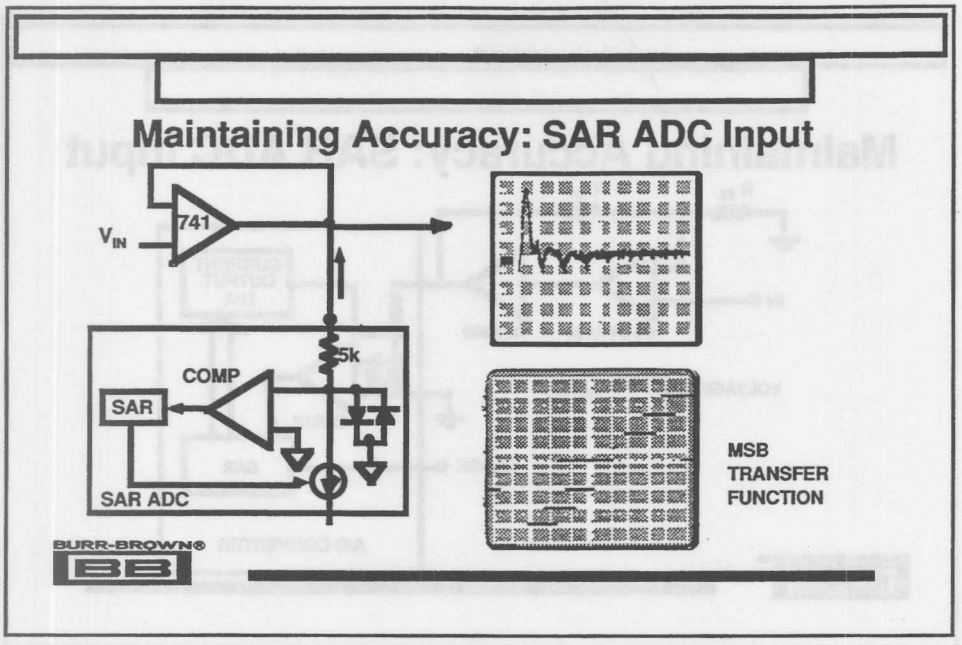
Maintaining Accuracy: Op Amp Gain Accuracy

This graph can be used to determine the closed-loop pole frequency necessary for a given level of accuracy, normalized to a signal frequency of 1.



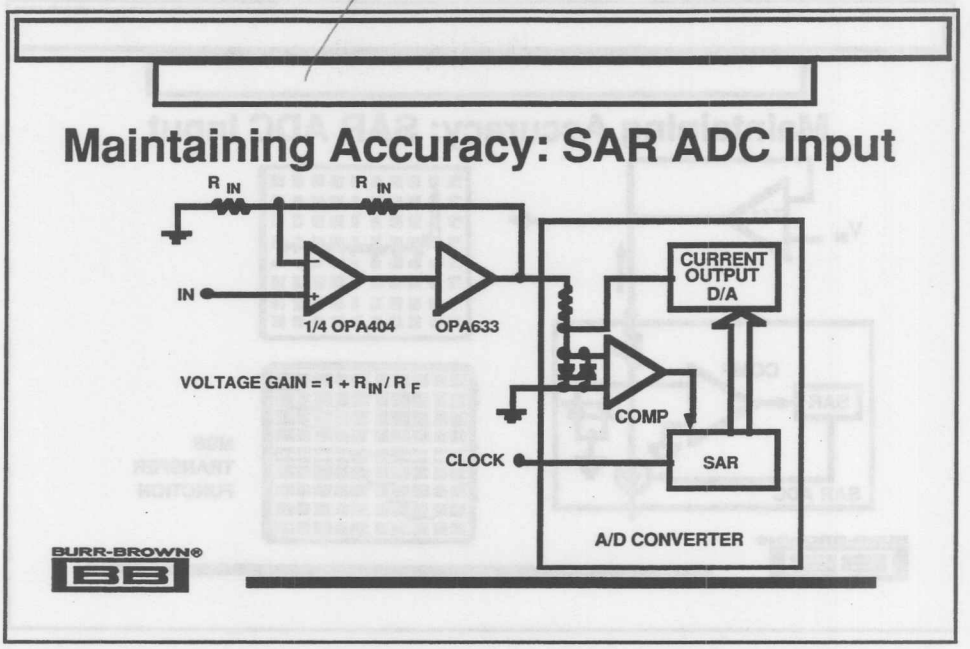
Maintaining Accuracy: SAR ADC Input

The input to a successive approximation converter presents the designer with a interesting problem. The input is tied to a point where the current or voltage may be changing rapidly as the DAC changes its output while the approximation process goes on. This presents a dynamic impedance to the circuitry driving the ADC. If this circuitry does not have a low output impedance over a wide frequency range, conversion errors may result.



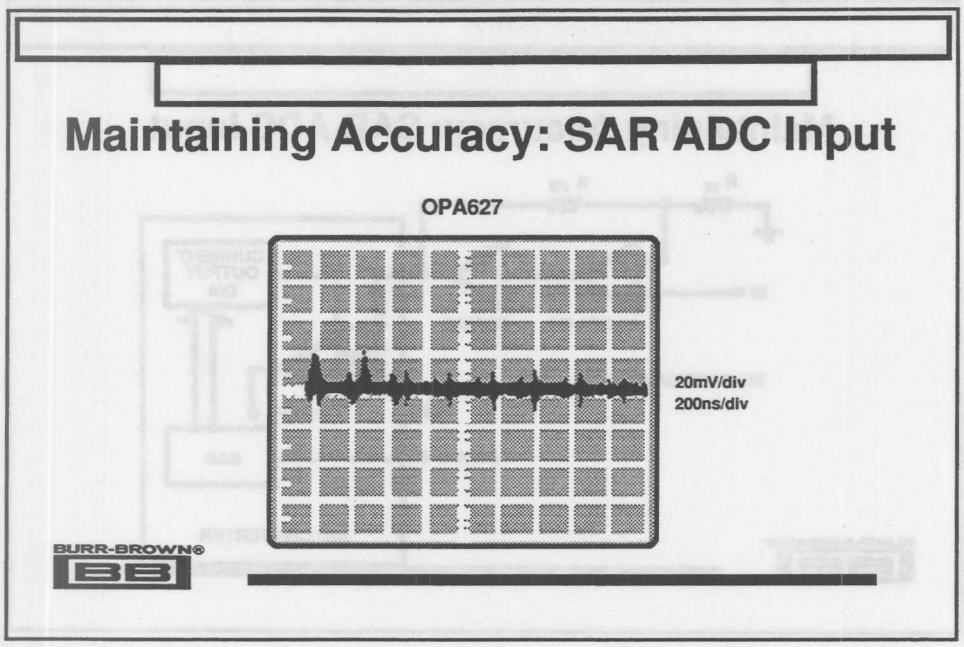
Maintaining Accuracy: SAR ADC Input

For example, driving a SAR ADC with an inexpensive "commodity" op amp such as 741 is NOT a good idea. As you can here, the output of the 741 "rings" excessively - but this is not due to a settling time problem.



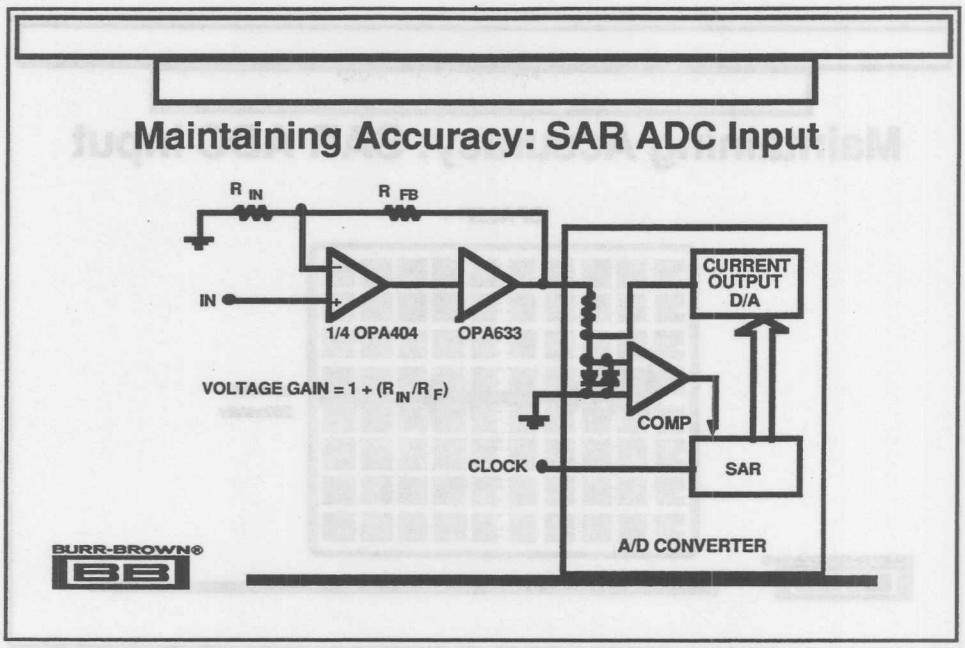
Maintaining Accuracy: SAR ADC Input

The problem is a result of the op amp's output impedance - which tends to become higher as the loop gain decreases. Most successive approximation converters operate at conversion speeds which are fairly fast - making a bit decision every 250nS to 1µS. This means the op amp must maintain a very low output impedance at frequencies of 1MHz to 4MHz.



Maintaining Accuracy: SAR ADC Input

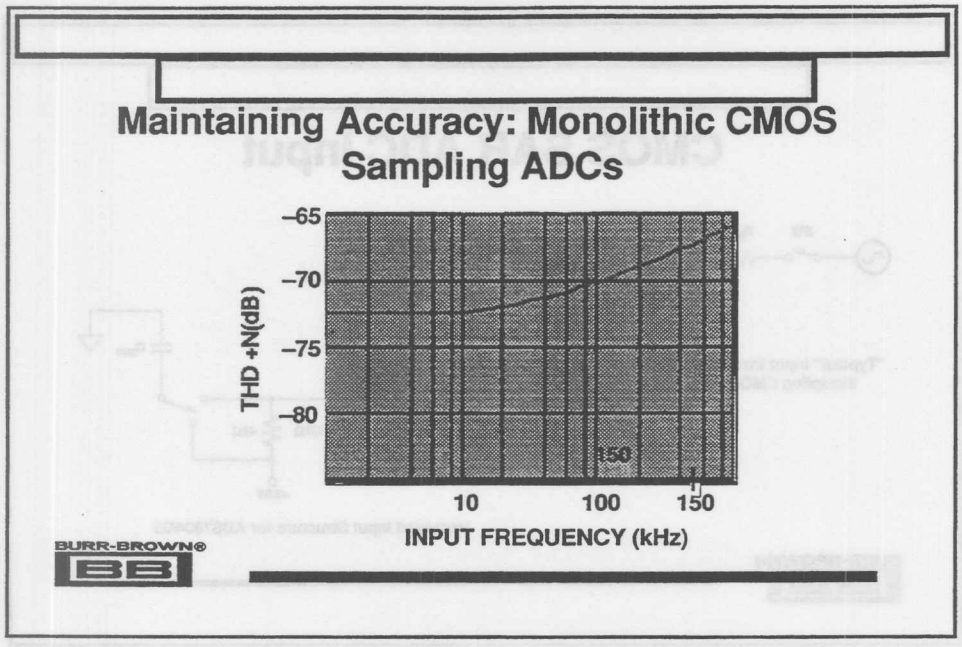
An op amp such as our OPA627 will provide a low output impedance at these frequencies. As you can see here, the "ringing" on the output of the OPA627 is very low by using this wideband amplifier.



Maintaining Accuracy: SAR ADC Input

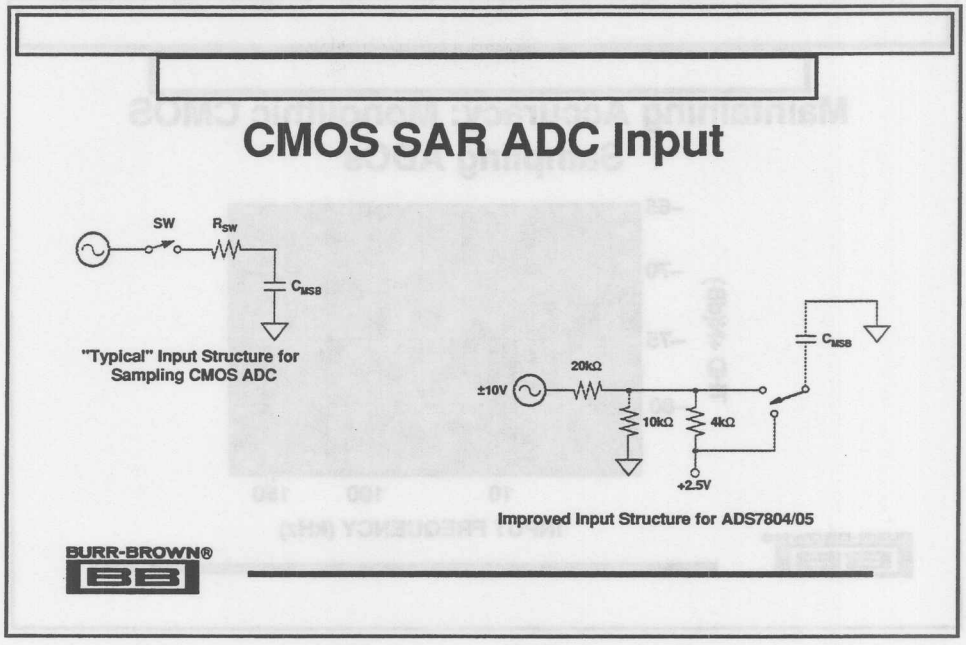
High resolution systems require precision amplifiers which, unfortunately, are likely to have low bandwidth. One unsatisfactory solution is to use a wide-band but perhaps less precise amplifier. Another solution is to add a high-speed unity-gain buffer stage to the output of the slower (but precision) amplifier, as shown here. A composite amplifier may also be used for greatest speed and precision (see Application Bulletin AB-007).

All this talk of op amps driving an ADC is valid, but generally these op amps are present inside of the sample/hold designed for use with the ADC in question. If you design your own sample/hold, however, you should be aware of these potential problems.



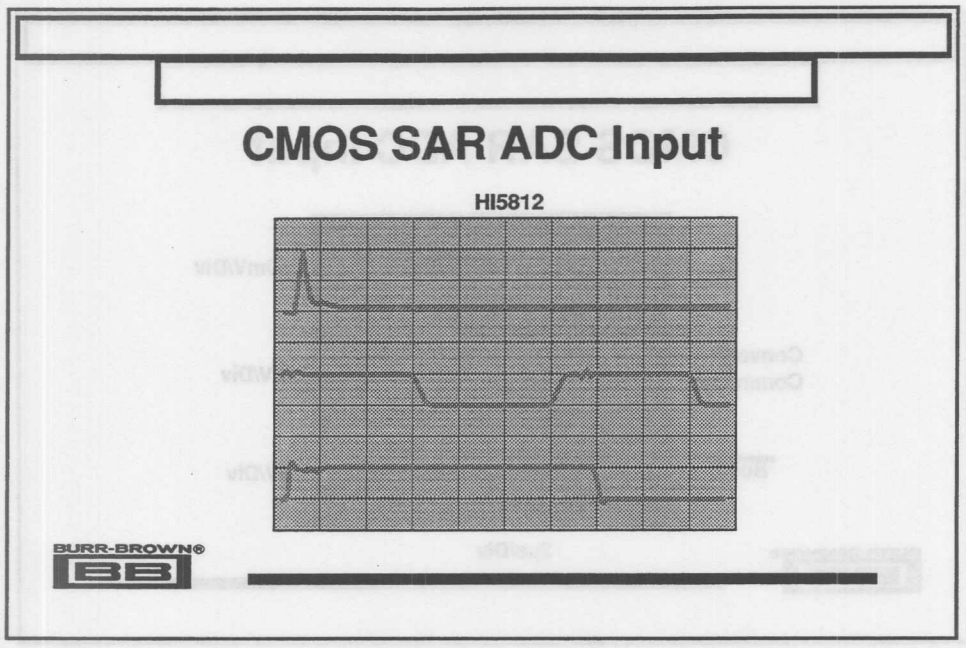
Maintaining Accuracy: Monolithic CMOS Sampling ADCs

ADCs which have their own sample/hold built-in, such as the sampling C-DAC based ADCs we looked at earlier, have their own performance limitations. In particular, these ADCs have some degradation in distortion performance as the signal frequency increases, as shown here for the ADS7800. This is due to nonlinearities in the FET switch used to connect the input signal to the C-DAC.



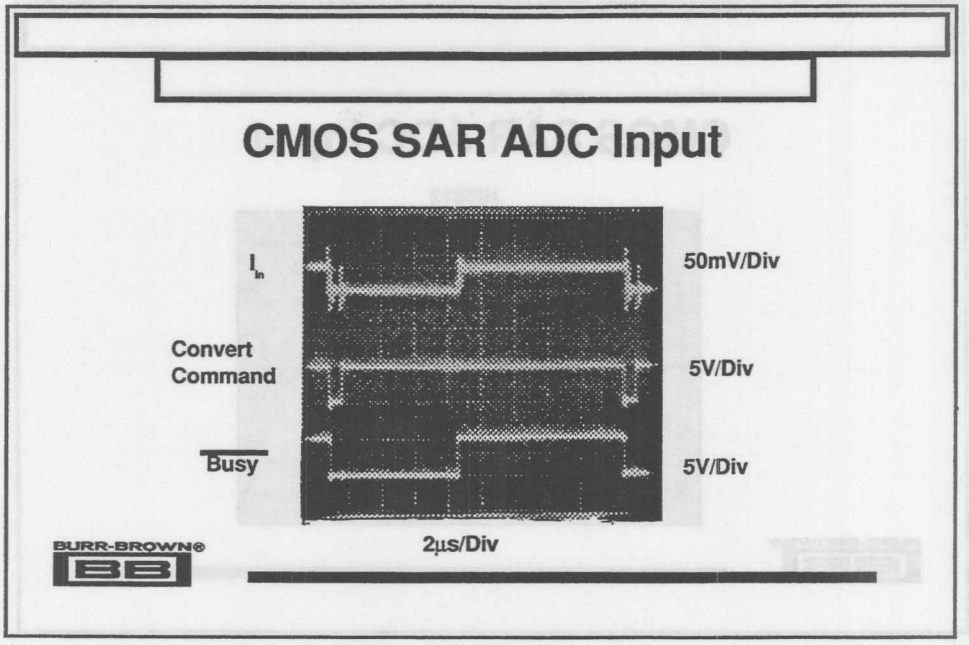
CMOS SAR ADC Input

Here we see typical input structures for two types of CMOS SAR ADCs. As we will demonstrate in the following two slides, the type of input structure can heavily influence the selection of an input buffer amplifier.



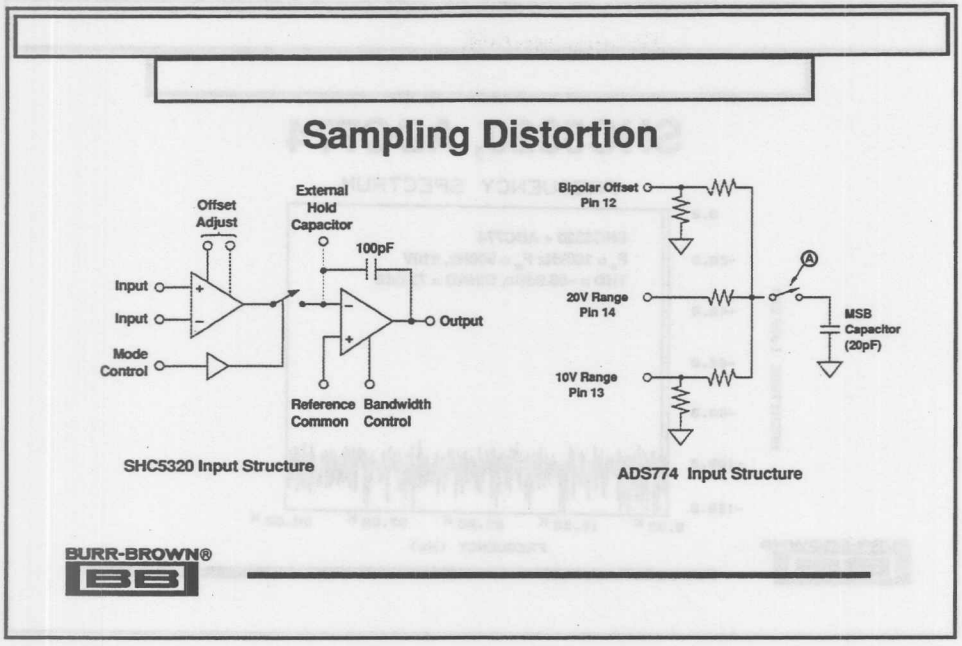
CMOS SAR ADC Input

A potential problem with CDAC based SAR converters can be charge released by the hold capacitor when the switch is moved from hold to track mode. This charge causes a current spike to appear at the input pin. The input source must have low enough impedance and enough drive capability to overcome the current spike. In the example shown above, a buffer amplifier with sufficient drive capability must be used.



CMOS SAR ADC Input

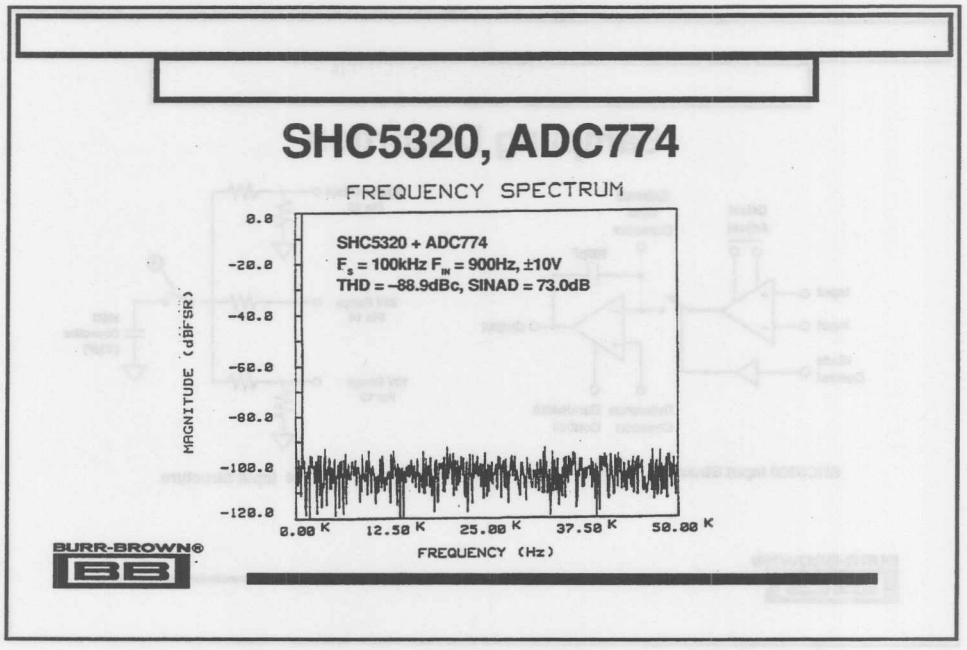
The ADS "family" recently introduced by Burr-Brown has solved the problem of charge being dumped back to the input pin by using a different input configuration. The ADS7806 shown above has a largely resistive input, so a buffer with low drive current, or no buffer at all is sufficient.



Sampling Distortion

Sampling distortion is normally dominated by the non-linearity of the input sampling mechanism as the input frequency changes. Until recently, a typical solution to sampling dynamic signals was to place a separate track-and-hold circuit on the front end of an ADC, such as a SHC5320. Now there are many CMOS ADCs available which have built-in track-and-hold circuits.

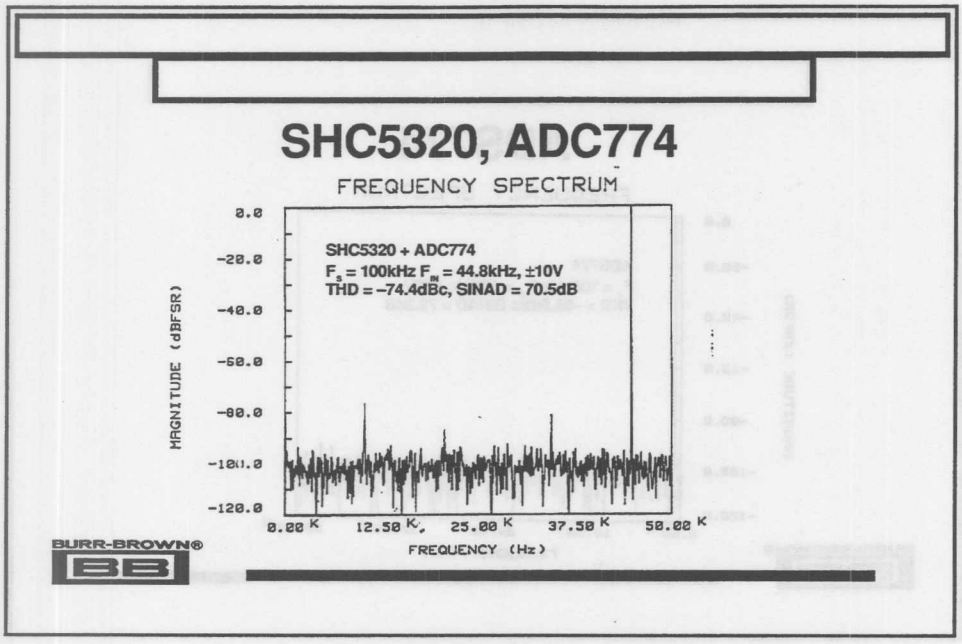
The diagram above details the input stages of a SHC5320 and a typical CMOS sampling ADC such as Burr-Brown's ADS774. In both cases, sampling distortion is dominated by the analog switch, "A". The linearity of this switch degrades with increasing input frequency.



SHC5320, ADC774

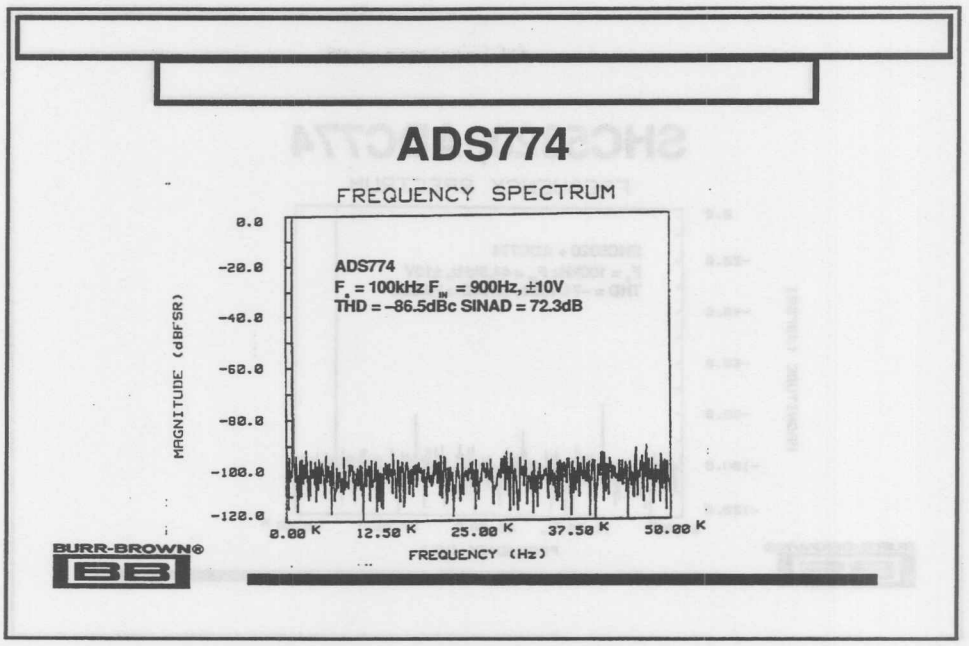
Now we'll examine how sampling distortion varies in terms of input frequency, input amplitude and architectural differences.

The first configuration we'll look at is the "classical" approach of placing a SCH5320 in front of an ADC774. This is an FFT plot of a 900Hz full-scale signal. The noise of the system dominates, with no frequency bin other than the fundamental pushing much out of the noise floor.



SHC5320, ADC774

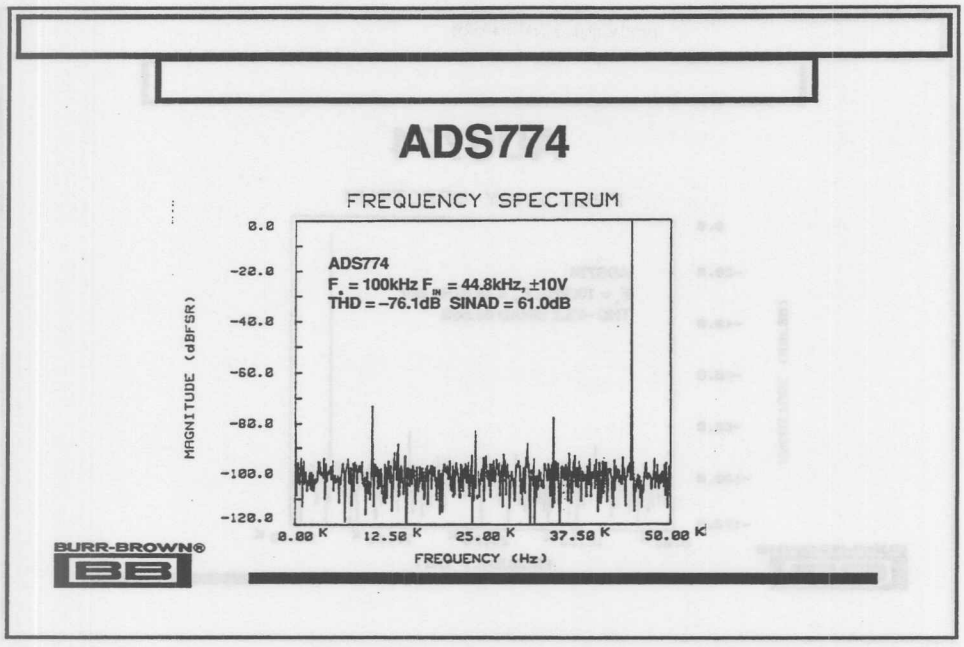
Now we look at the same configuration with an input frequency close to Nyquist at 44.8kHz. The second, third and fourth harmonics of the fundamental clearly show up above the noise floor, aliased into bins near 10kHz, 35Hz and 20kHz respectively.



ADS774

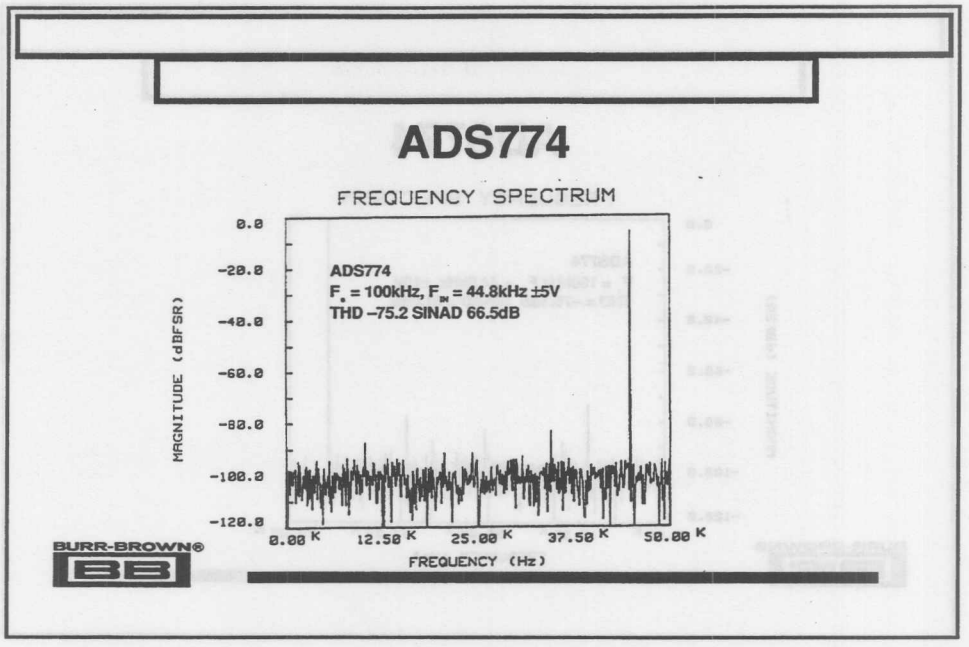
The next configuration is a CMOS sampling ADC, Burr-Brown's ADS774. This converter uses a switched-capacitor array, which samples by capturing a charge proportional to the input voltage on the MSB capacitor. This approach allowed power to be decreased by 88% (from 660mW to 75mW) yet still has performance close to the two-chip higher power solution of SHC5320 and ADC774.

Total Harmonic Distortion for a 900Hz input signal for the ADS774 is 86.5dB below the fundamental.



ADS774

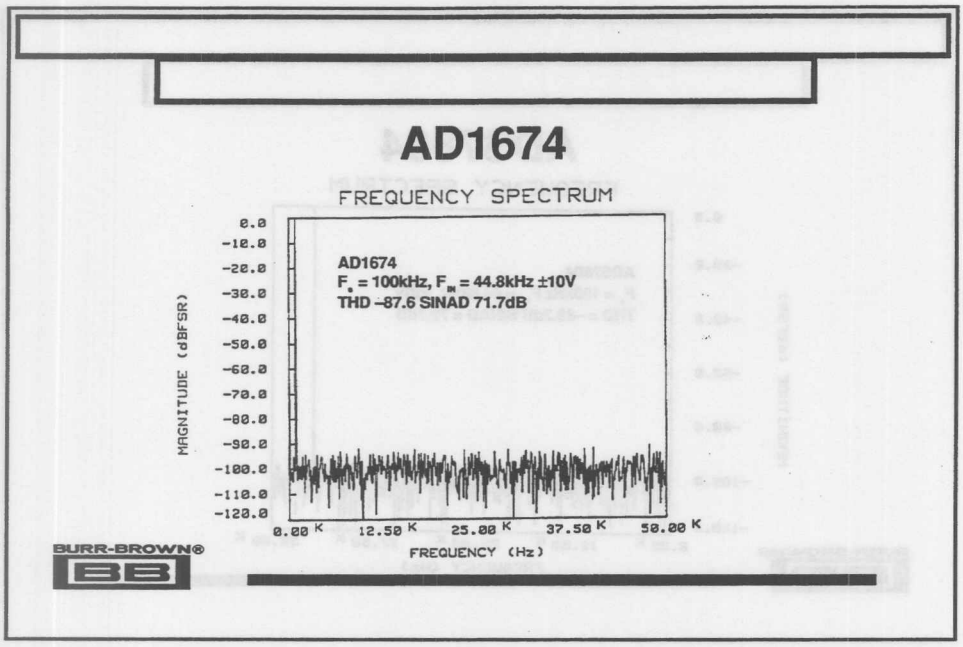
Now we look at ADS774 with a near Nyquist input. Similar to the two-chip solution, dynamic performance has degraded, showing the effect of sampling distortion. This approach shows a difference of 3 to 5dB worse than the SHC5320 + ADC774 combo, but the price/power ratio make it an extremely attractive choice.



ADS774

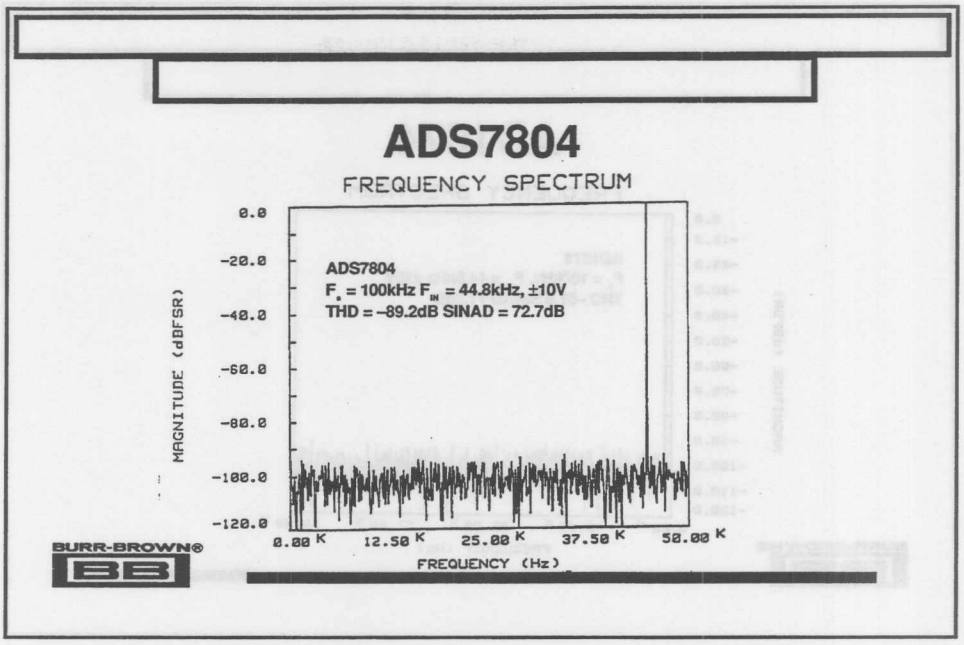
We have some approaches for reducing sampling distortion. The first is to simply reduce the input range to the ADC. This reduces the maximum slew rate from any particular input frequency, which reduces the non-linearity of the sampling mechanism. Depending on the application, the resulting decrease in available dynamic range may be offset by an increased usable SFDR over a wider input frequency range.

This plot shows an ADS774 with the input amplitude reduced by 6dB. This approach improves THD from –70.5dBc (full-scale input) to –75.2dBc. SFDR has also increased, from 72.8dB to 83.4dB. Since the input has been reduced by 6dB, this indicates an effective 4dB in dynamic range can be achieved.



AD1674

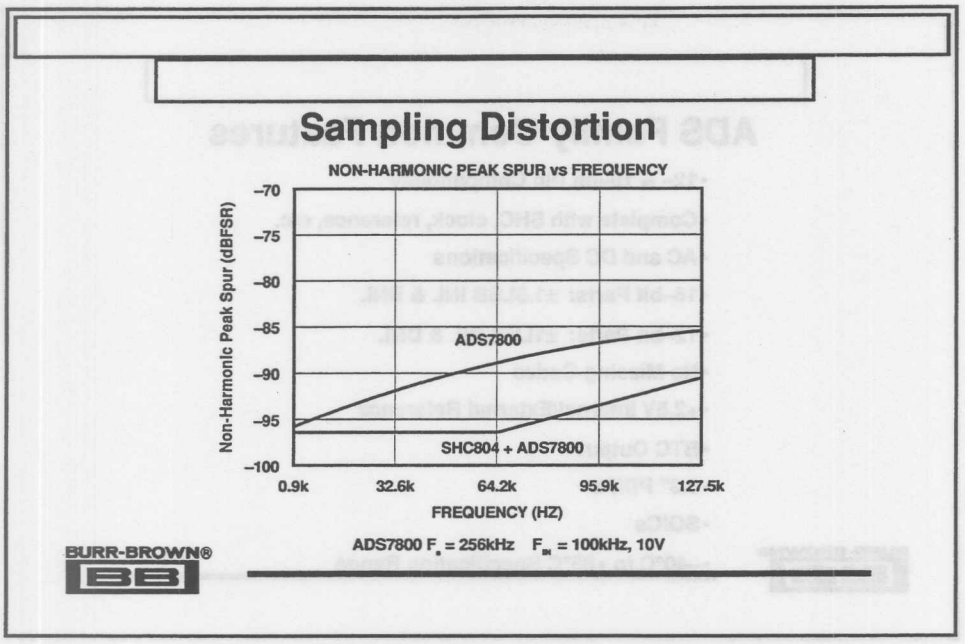
Another approach to reducing sampling distortion can be realized by using other sampling ADCs. If system power is not critical, some improvements in distortion may be obtained through using a BiCMOS ADS, such as Analog Devices' AD1674. This plot shows the AD1674 with a near-Nyquist input signal. This part performs well, with only the second harmonic rising out of the noise floor.



ADS7804

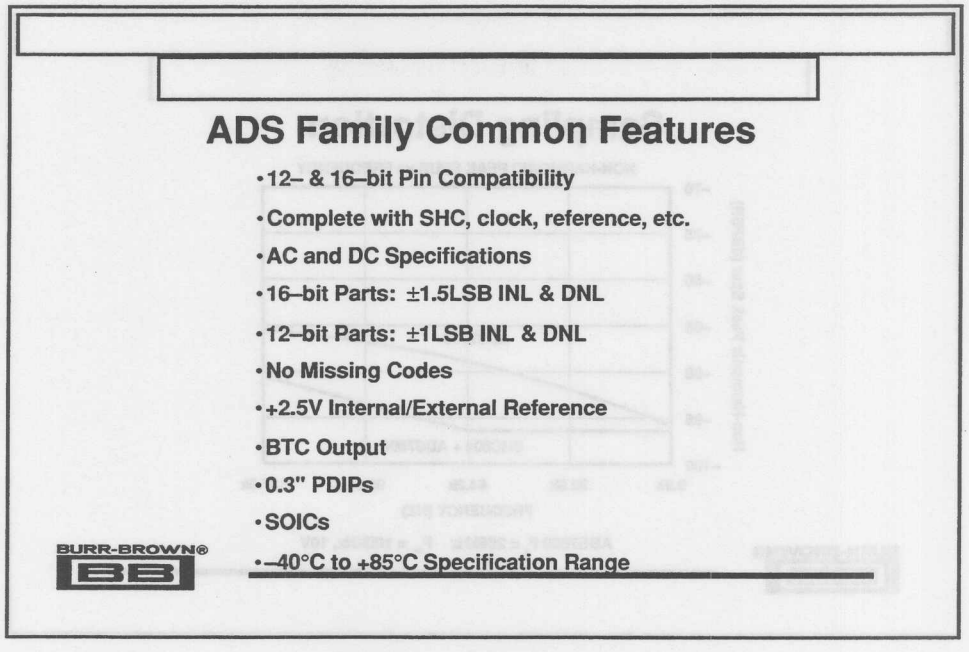
Experience with the input structure of the ADS774 has allowed Burr-Brown to develop the next-generation CMOS ADC family, with performance exceeding comparable BiCMOS parts at a fraction of the power and price of typical BiCMOS parts. One of the major changes between ADS774 and ADS7804 (FFT results shown above) was to significantly increase the size of the input switch. This reduces the on-resistance of the switch which reduces the effects of any frequency-dependent non-linearity.

The ADS 7804 results shown here demonstrate the best performance levels available in terms of distortion at a very attractive price/power combination.



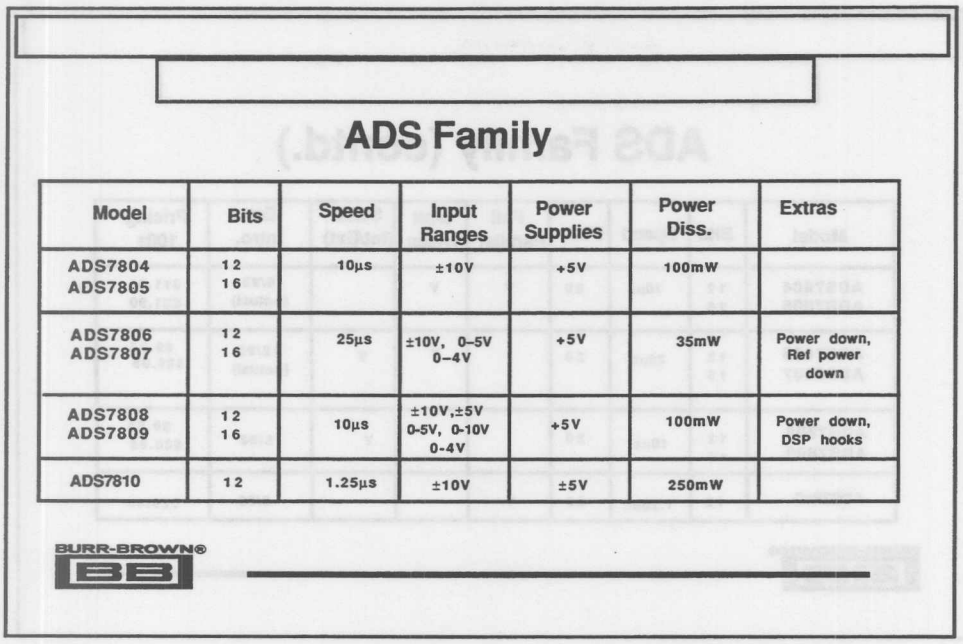
Sampling Distortion

If premium performance is required, another possible option is to place a spearate track-and-hold unit in front of a sampling ADC. The main drawback to this approach is added cost. The above example shows the improvement gained by placing a high-speed low-distortion T/H unit such as SHC804 in front of a high speed sampling ADC such as ADS7800. Using the external SHC804 means the sampling mechanism of the ADS7800 sees essentially DC, which results in an improved THD. For lower cost and higher speed requirements, SHC605 will also cause large improvements in distortion when placed in front of a sampling ADC.



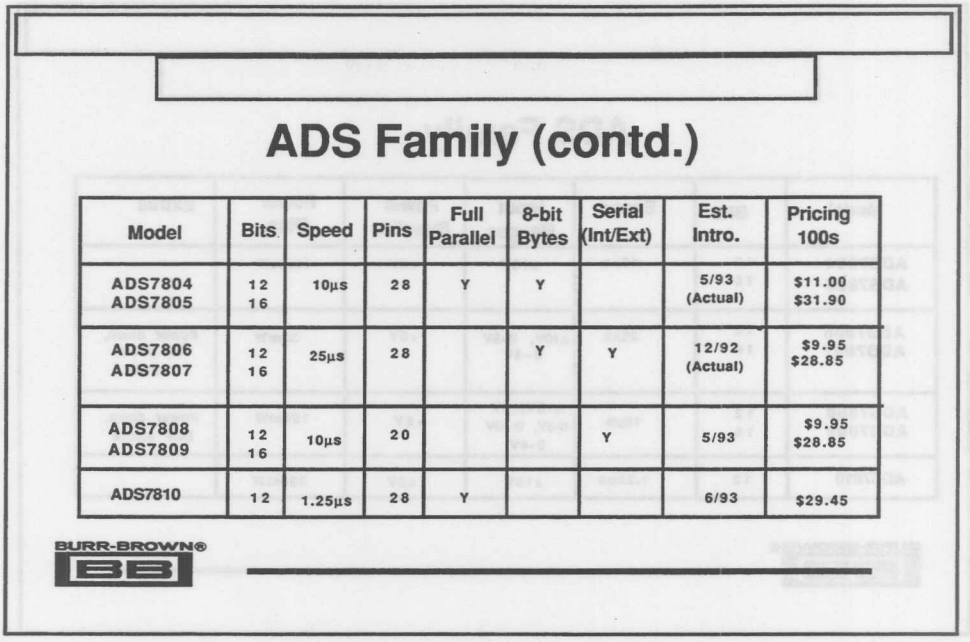
ADS Family Common Features

Burr-Brown has recently introduced a family of sampling CMOS A/D converters which constitute the next generation of general purpose "industrial" type sampling ADCs. Common features of the family are shown in the above slide.



ADS Family

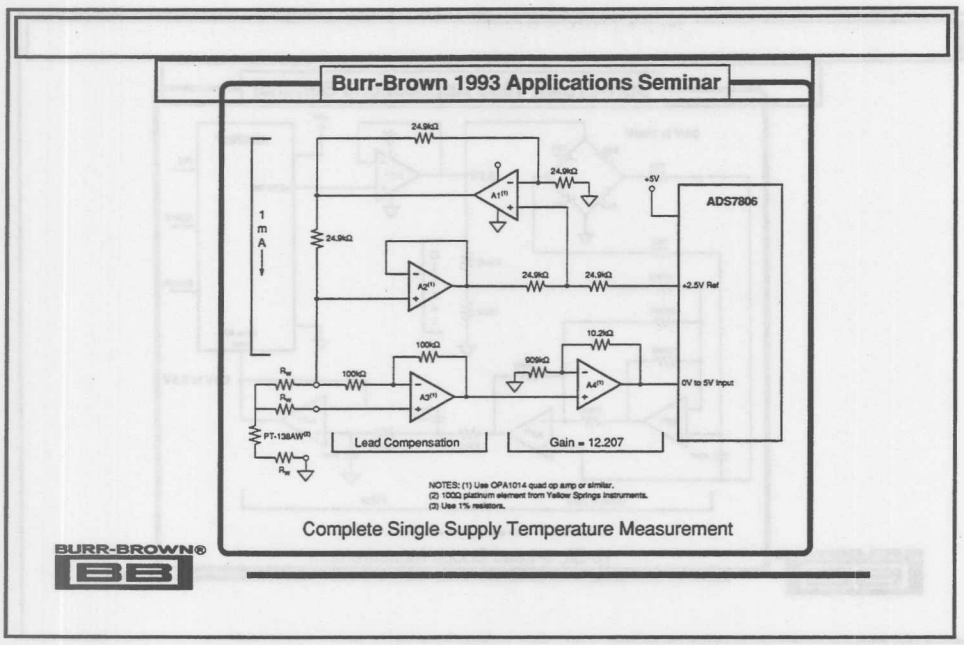
The ADS7804—7809 all use a single +5V power supply, and the ADS7810 uses ±5V supplies. The inputs have been configured to accept standard input ranges such as ±10V, 0 to +10V, ±5V, etc. These input ranges give the user a great deal of flexibility for a converter which requires only a single supply.



Model	Bits	Speed	Pins	Full Parallel	8-bit Bytes	Serial (Int/Ext)	Est. Intro.	Pricing 100s
ADS7804 ADS7805	12 16	10µs	28	Y	Y		5/93 (Actual)	$11.00 $31.90
ADS7806 ADS7807	12 16	25µs	28		Y	Y	12/92 (Actual)	$9.95 $28.85
ADS7808 ADS7809	12 16	10µs	20			Y	5/93	$9.95 $28.85
ADS7810	12	1.25µs	28	Y			6/93	$29.45

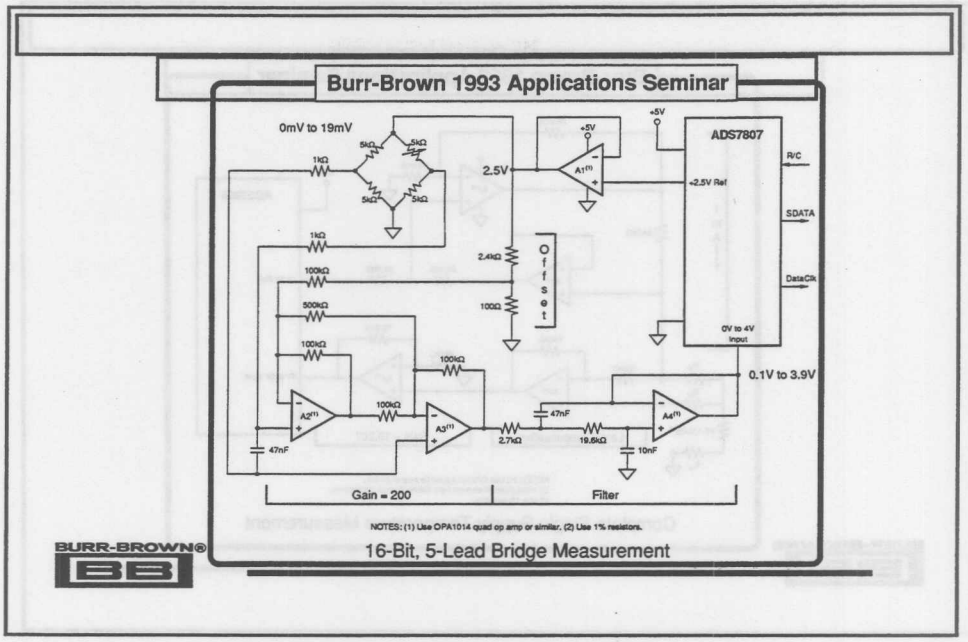
ADS Family (contd.)

All of the members of the ADS family are available in "skinny" 0.3" wide plastic DIP packages as well as standard SOIC versions. Also, flexibility has been provided with the output formats, offering versions in both serial and parallel formats.



Complete Single Supply Temperature Measurement

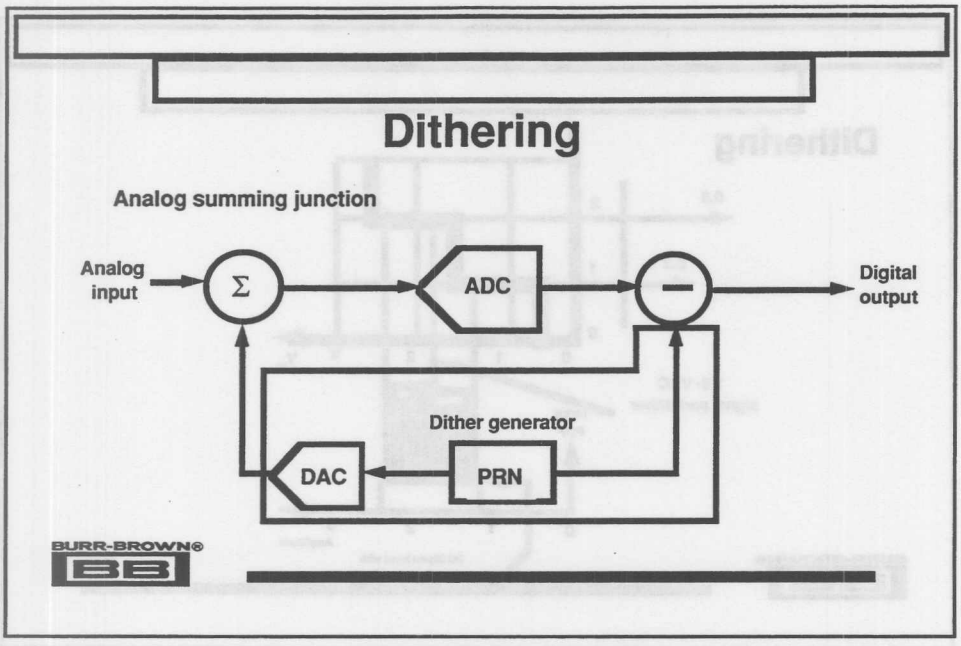
The 2.5V reference on the ADS7806 and two op-amps generate a 1mA current to excite the thermistor. A 0.1°C change in temperature generates a 1 bit change at the output of the converters using the standard 1% resistors shown. Total power will be less than 40mW for this complete sampling system.



16-Bit, 5-Lead Bridge Measurement

The single active bridge element is excited by a buffered 2.5V generated by the converter's internal reference. Using 0—4V input range on the 16-bit ADS7807 offers headroom for the op-amps when using a single +5V supply.

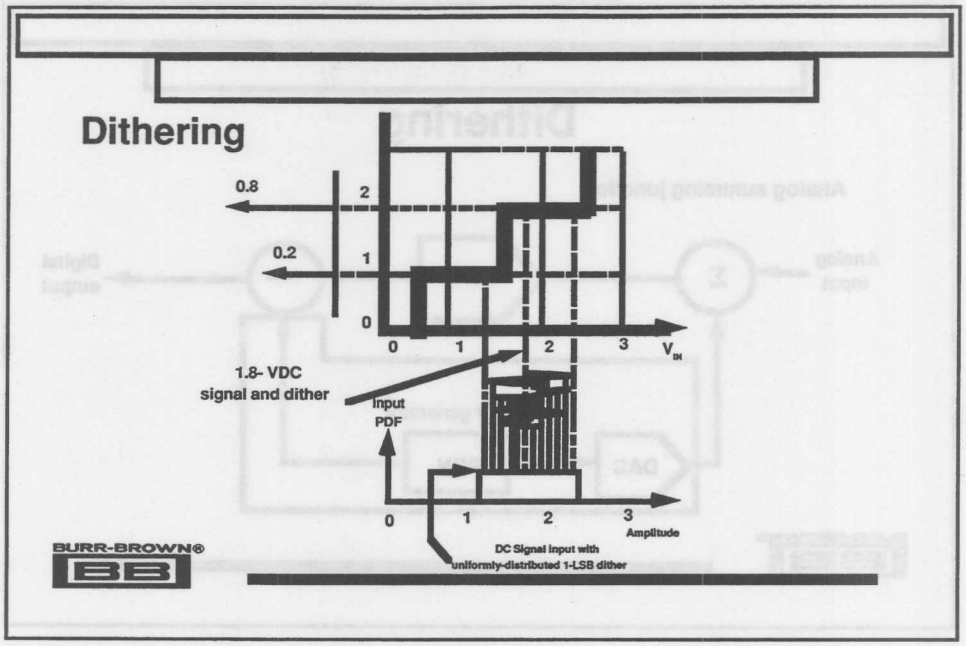
Using the ADS7807 serial output in the internal clock mode allows simple isolation. The converter only outputs clock pulses when data is being transmitted, so that a single dual optocoupler could provide fully isolated 16-bit data. Total power will be less than 40mW for this complete sampling system.



Dithering

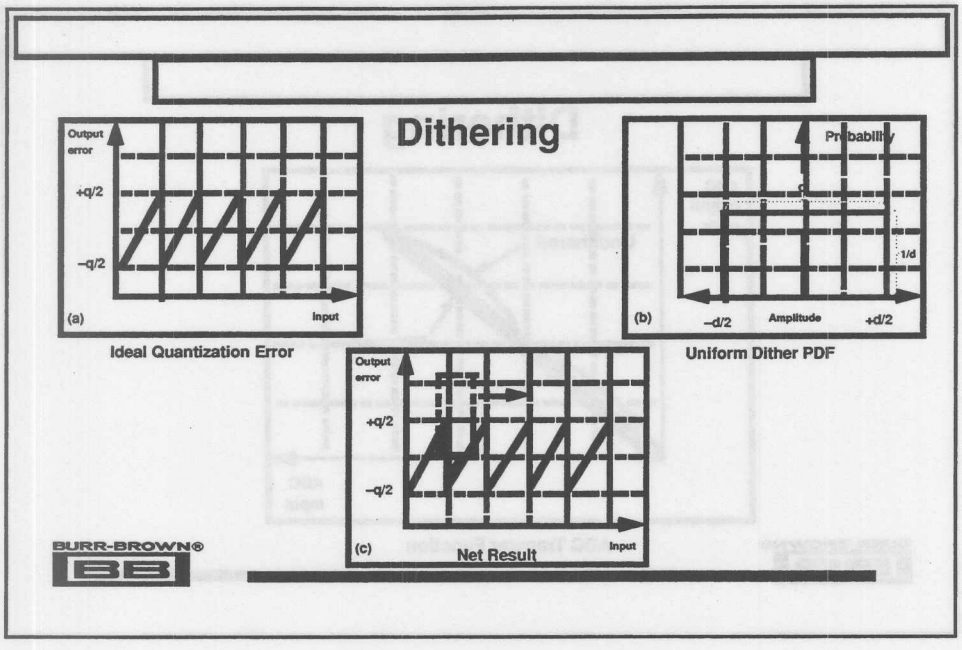
Dynamic range and noise performance of high-speed, high-resolution ADCs can be improved through large-scale dithering. Dithering is a method for randomizing an ADC's quantization errors by adding uncorrelated noise or stimulus to the analog input.

In the externally - dithered ADC application shown above, the dither amplitudes must be subtracted digitally at the output to avoid compromising SNR. The dither signal consists of a uniformly distributed random noise generated by a pseudorandom number generator.



Dithering

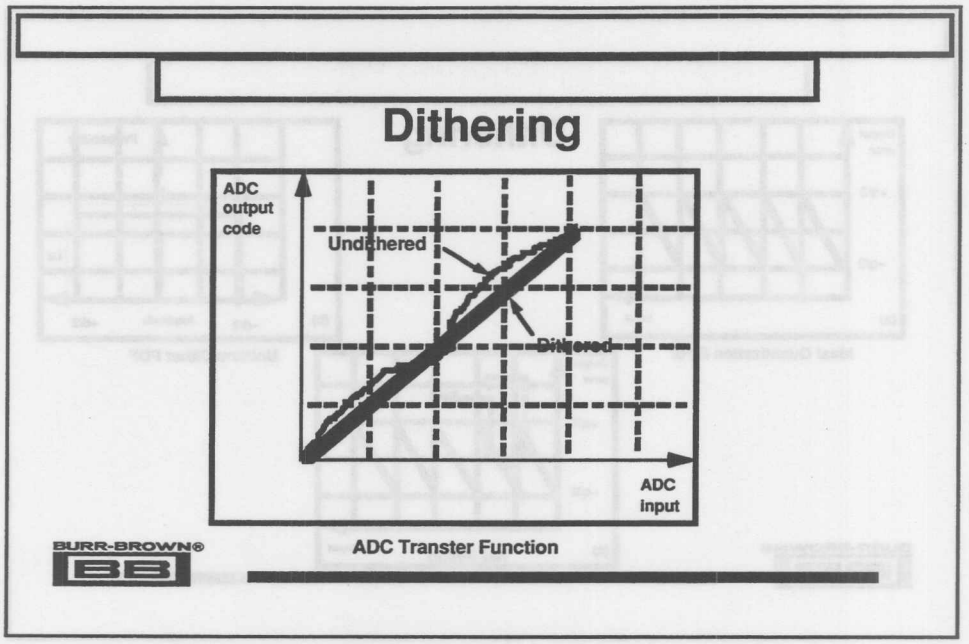
If the input signal is added to a random noise stimulus of uniform PDF and one LSB amplitude, the output will change between code values. The digital output can then be time-averaged or filtered to allow for extraction of an amplitude of less than one LSB stop size. This technique can be used to drastically reduce quantization errors.



Dithering

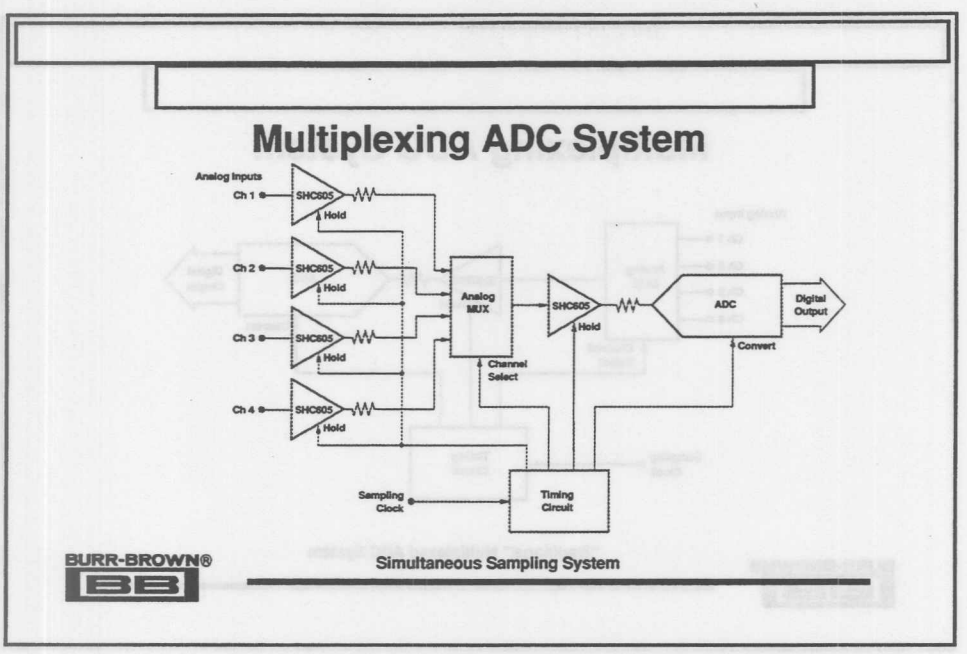
For an ideal transfer function, the quantization errors in the average transfer function resulting from the dither go to zero if the small-scale dither amplitude approaches one LSB in magnitude. This occurs for uniform dither of amplitudes equal to an integral number of LSBs for an ideal ADC transfer characteristic.

Figure c shows how a and b, when integrated together, yield a total area product which sums to zero for any position during the convolution.



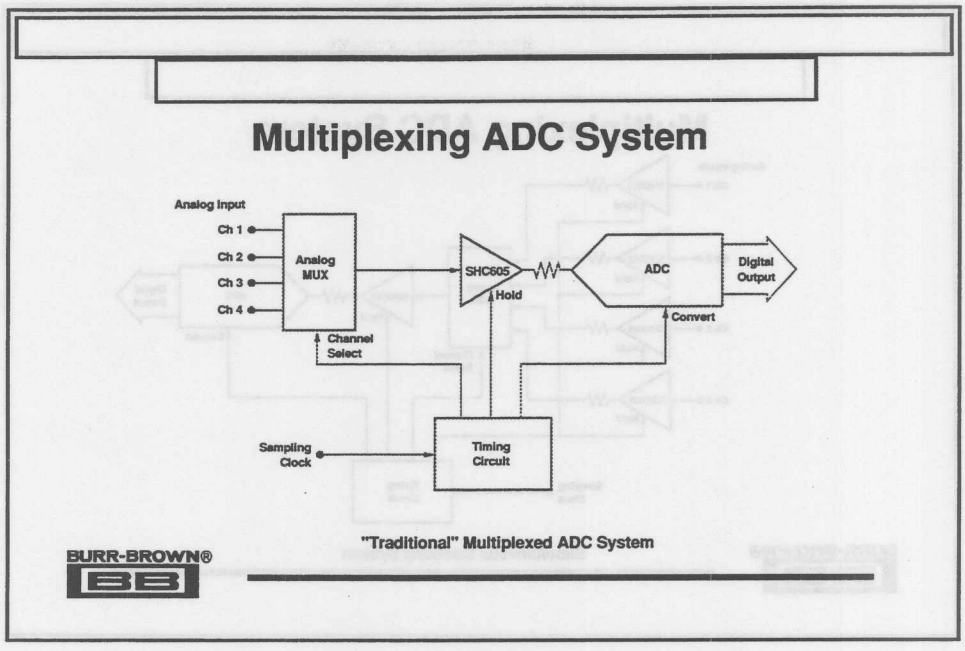
Dithering

For dither amplitude much greater than one LSB, lower order distortion is smoothed out. Such large-scale dithering improves transfer functions whose Taylor series expansion include higher-order terms. The degree of low-order distortion improvement is directly related to the magnitude of the dither signal.



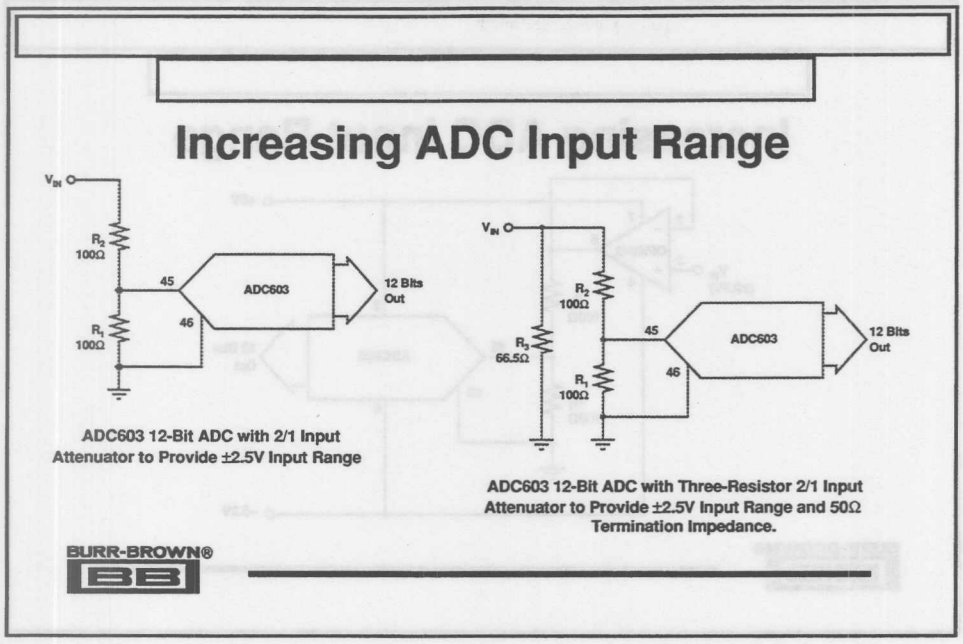
Multiplexing ADC System

A different approach for multiplexing is simultaneous sampling. In this case, the input T/H circuits go into hold mode at the same time. The ADC will then poll them in order, and the result is a "snapshot" in time of an event. One caution when using this approach - many monolithic high-speed T/H circuits have high droop rates, which can cause accuracy errors. Be certain to include these errors in your budget, as well as channel-to-channel accuracy variations.



Multiplexing ADC System

Another way to get more performance from your ADC is to use higher speed converters in a multiplexed system. This can also lower system cost, especially as technology advances lower the price of high-speed high-resolution ADCs and T/H circuits. The above system shows a "traditional" approach, where multiple channels are being "polled" by the ADC. This is an excellent approach when speed-per-channel is not of great concern.

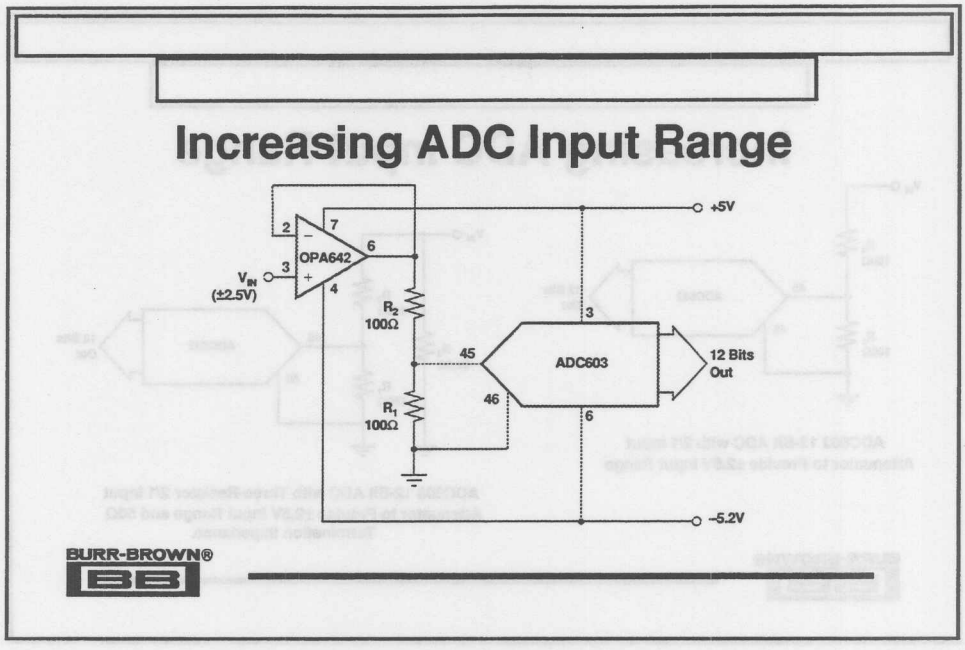


Increasing ADC Input Range

A problem faced with many of the high-speed ADCs available today is limited input range. To obtain the necesary speed, advanced processes using 5V power supplies are required. Common input ranges for such ADCs are ±1.25V and ±1V.

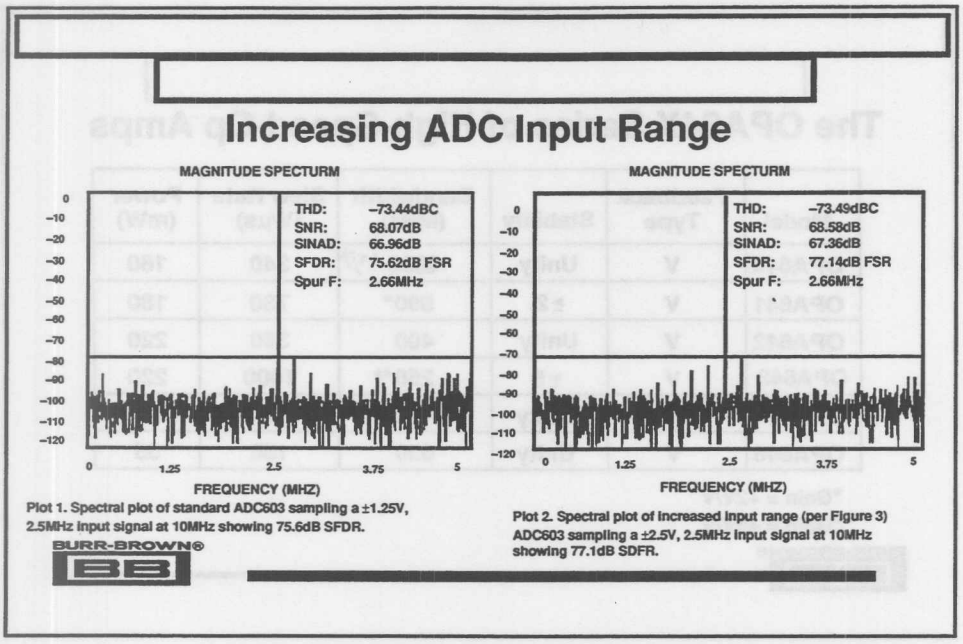
The first circuit shown is a simple resistor divider. The source impedance of the divider is R_1 in parallel with R_2. A source impedance of 50Ω is recommended. If higher divider impedances are needed and adding a buffer is not viable, source impedances up to 500Ω can be used.

The second circuit is used when 50Ω termination is required. The three-resistor approach improves accuracy by placing the majority of the termination power dissipation in the third resistor. This minimizes self-heating effects in the divider network.



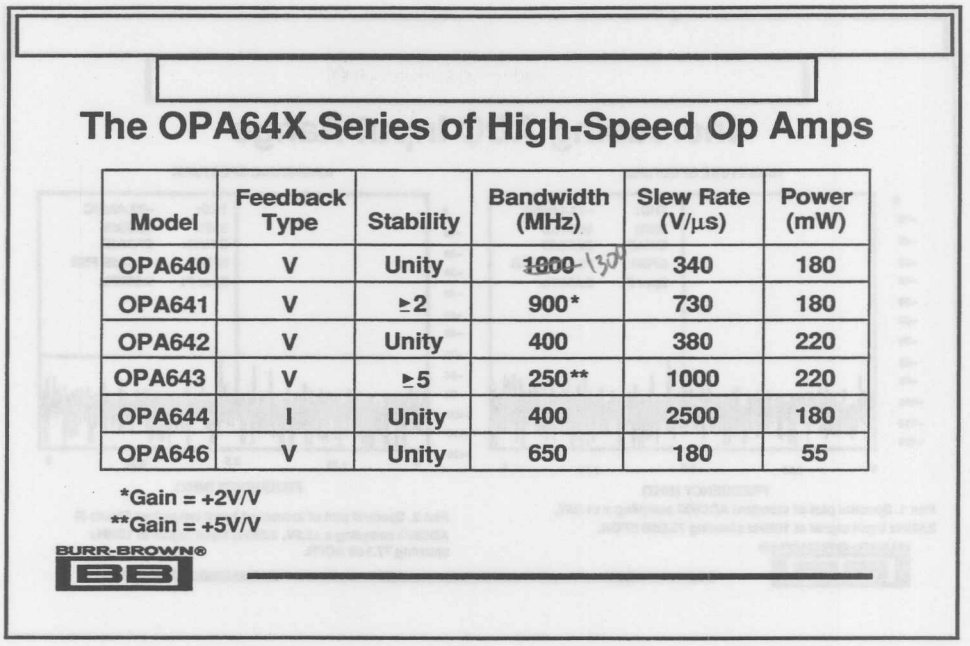
Increasing ADC Input Range

If a high input impedance is required, drive the divider with a unity-gain-connected, high-speed, low-noise op-amp such as Burr-Brown OPA642 as shown above. The OPA642 can be used for inputs as high as ±3V.



Increasing ADC Input Range

These spectral plots compare a standard 1.25V input ADC603 to a 2.5V input, OPA642 buffered ADC603 as previously shown. The results show the SFDR of the boosted circuit is as good, if not better, than the standard circuit. The slight improvement is due to being driven from a purely resistive source, as opposed to the complex impedance of the cable and signal generator.



The OPA64X Series of High-Speed Op Amps

Burr-Brown's new series of operational amplifiers offer extremely high-speed in a variety of configurations.

The OPA64X Series of High-Speed Op Amps

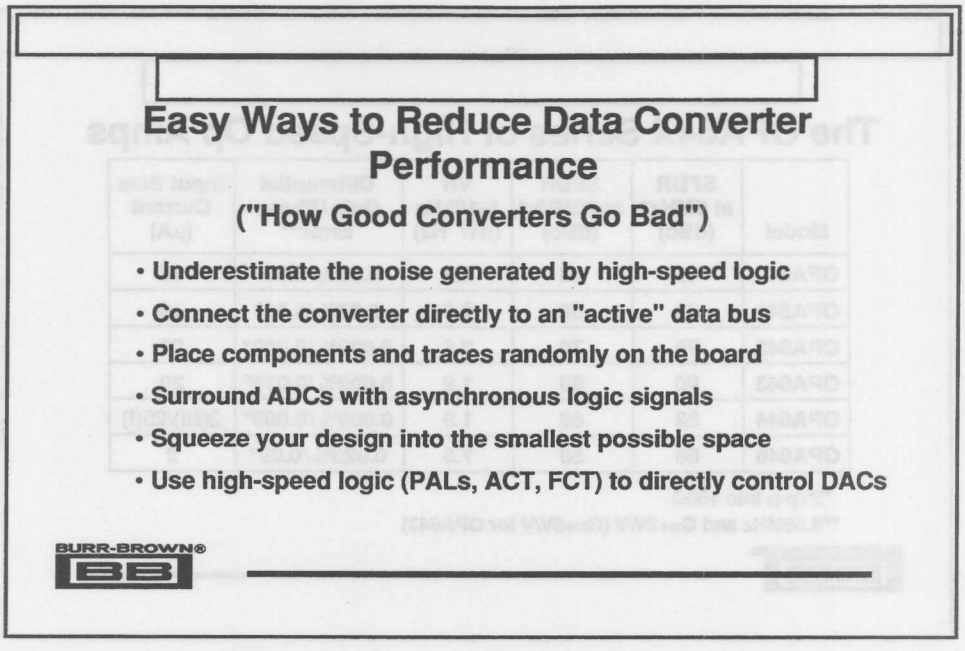
Model	SFDR at 5MHz* (dBc)	SFDR at 20MHz* (dBc)	VN f=10kHz (nV/ Hz)	Differential Gain/Phase Error**	Input Bias Current (μA)
OPA640	85	63	2.8	0.06%/0.01°	16
OPA641	83	66	2.8	0.07%/0.01°	16
OPA642	95	70	2.5	0.009%/0.008°	20
OPA643	90	68	1.9	0.009%/0.015°	20
OPA644	82	68	1.9	0.009%/0.009°	2(NI)/25(I)
OPA646	68	50	7.5	0.025%/0.09°	2

*2Vp-p into 100Ω
**3.58MHz and G=+2V/V (G=+5V/V for OPA643)

BURR-BROWN®

The OPA64X Series of High-Speed Op Amps

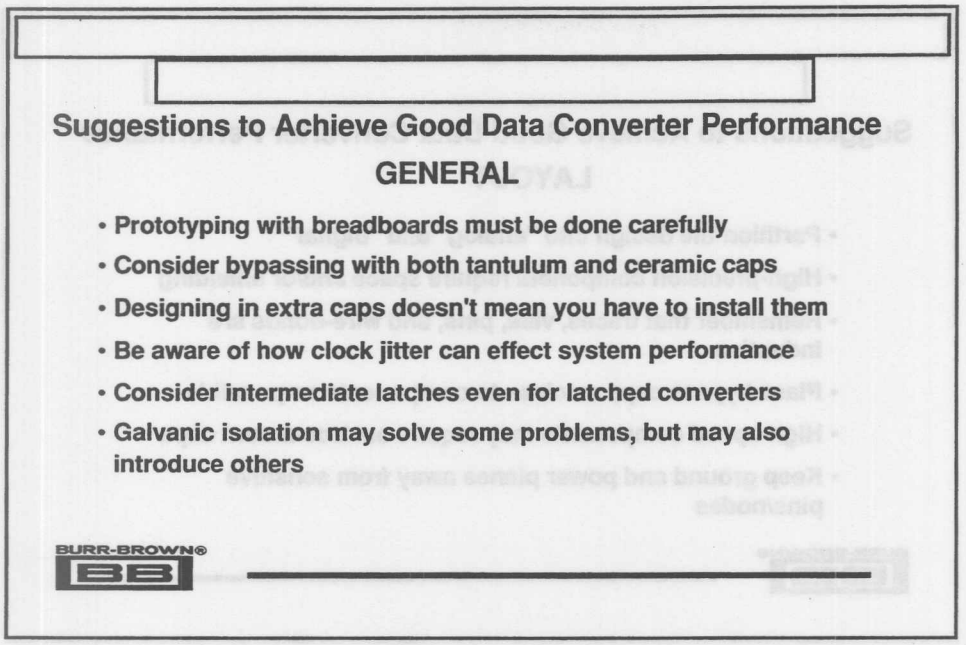
Burr-Brown's new series of high-speed operational amplifiers also offer excellent spurious-free dynamic range, low noise, and exceptional differential gain/phase error. Many designs—not only high-speed designs—may benefit from increased performance in these parameters.



Easy Ways to Reduce Data Converter Performance

There are many ways to reduce the performance on analog-to-digital and digital-to-analog converters. Most designers will be aware of at least a few of these (including those that found out the hard way). The items covered here are those that seem to occur most often in modern designs.

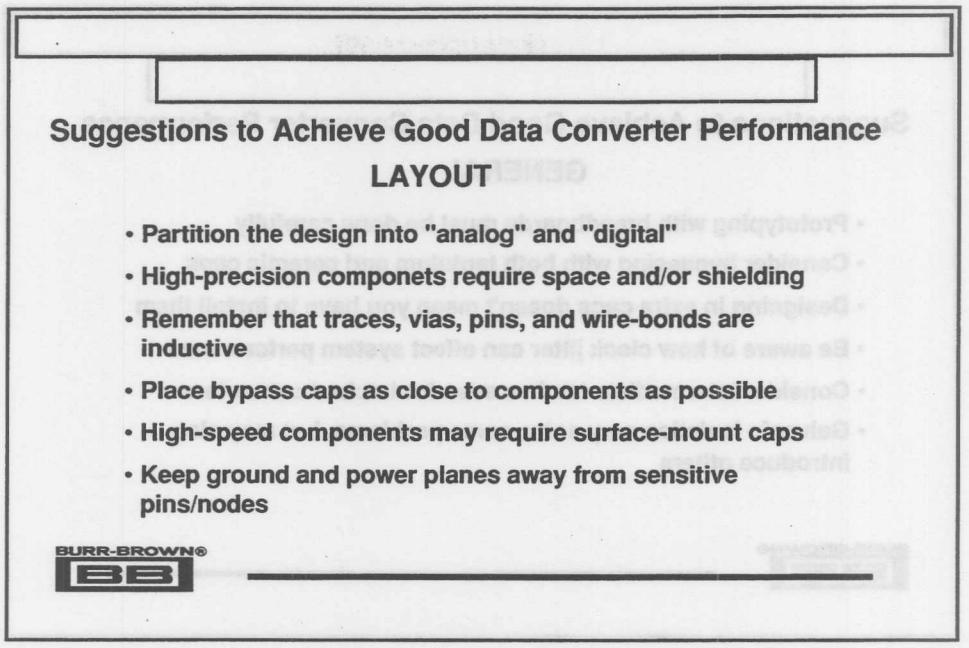
Notice that many of the items are in direct conflict with common "digital design" practices. Modern digital designs place emphasis on fewer components (even if there are more total transistors), higher speed, smaller board size, multiple clocks of various frequencies, and automated board placement and routing. Using this approach with analog or mixed-signal components will almost certainly mean reduced performance.



Suggestions to Achieve Good Data Converter Performance

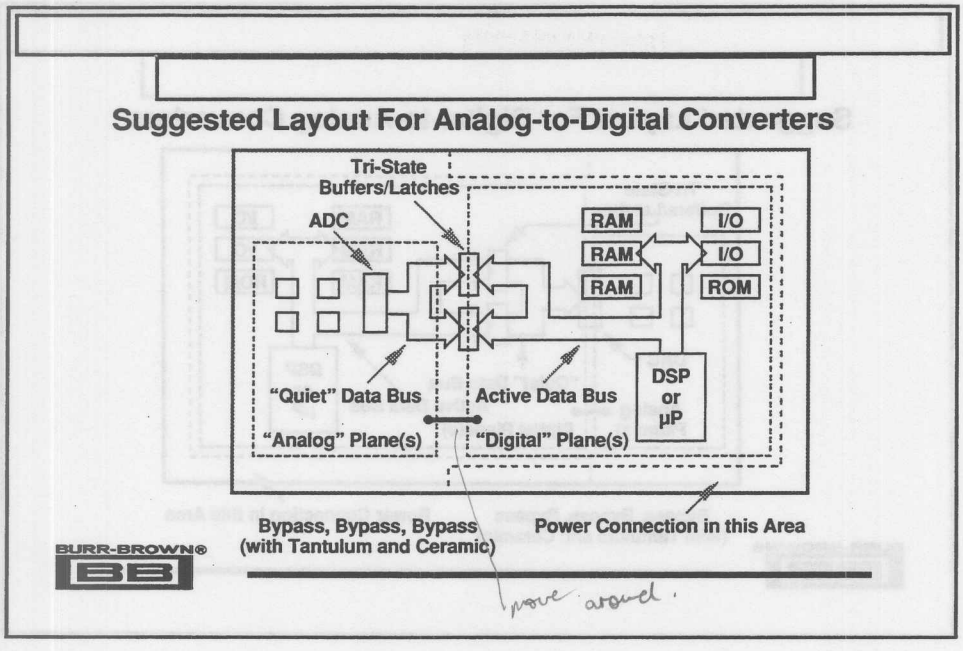
Here are some general guidelines to achieving good performance from data converters. Some of these items are discussed in more detail elsewhere in the seminar. When designing with high-precision and high-speed components, keep in mind that each design is unique. There are few "hard" rules—mostly just general guidelines.

If your design requires the absolute best performance from a data converter and the converter is high-precision (or "high-precision" at high-speed—12-bits at 10MHz, for example), then anticipate a "shake-out" phase. In this phase, you will need to try different configurations and verify the results. This means you need to make the board as flexible as possible, and will need some way to test the converters performance. Obviously, both of these can be difficult.



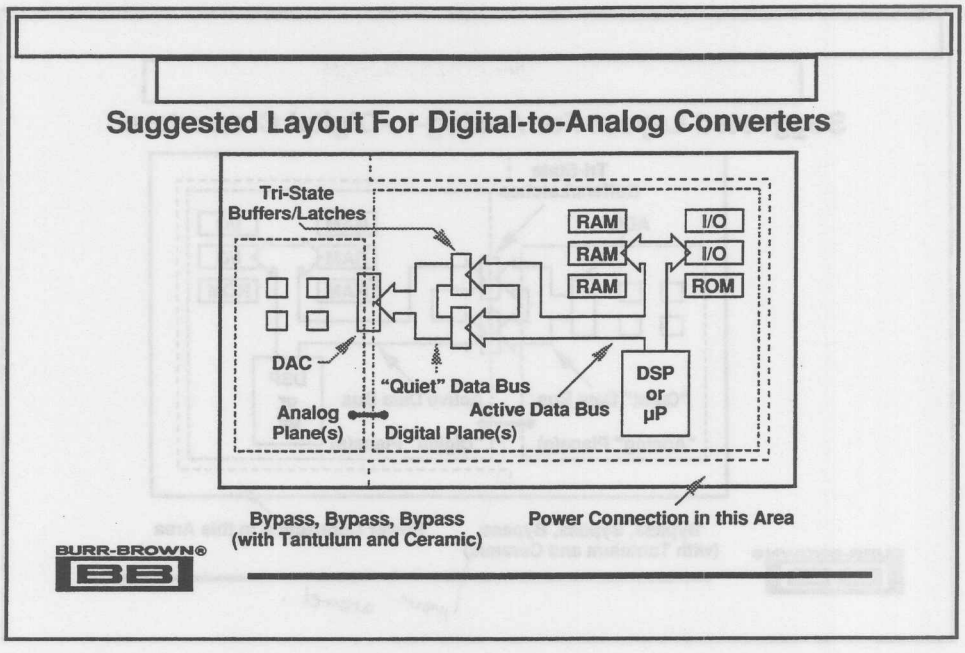
Suggestions to Achieve Good Data Converter Performance

This slide should be intitled "The Zen of Layout" since there are no concrete recommendations here. Designs are simply to varied to give any hard rules about layout. These guidelines should be used as an approach to the overall layout and be kept in mind during the layout process. When it comes to layout, there is no substitute for experience.



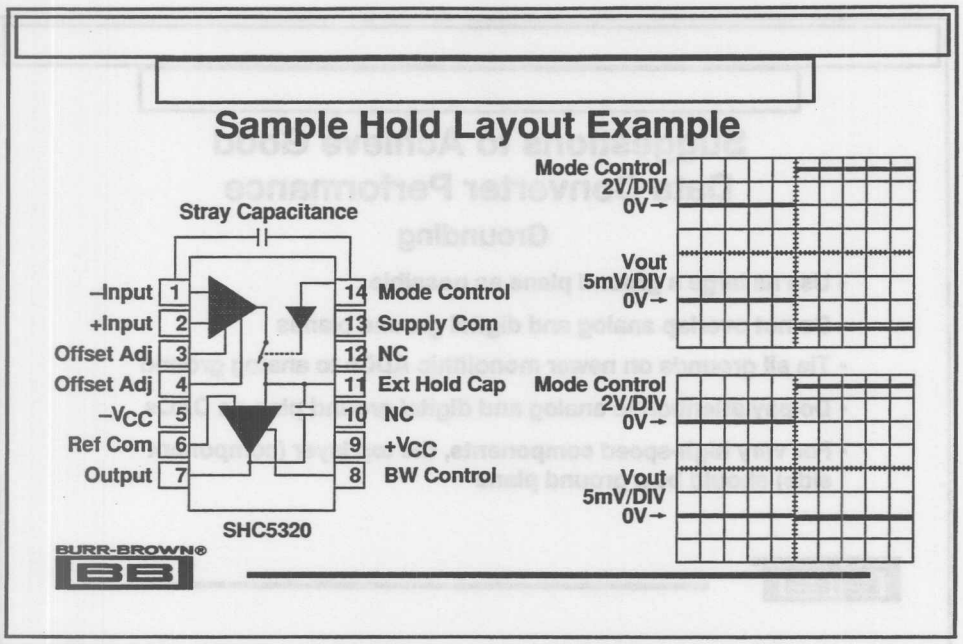
Suggested Layout For Analog-to-Digital Converters

This is the bare essence of laying out a board for modern, monolithic analog-to-digital converters. For older converters or for delta-sigma converters, a better layout might resemble the layout for a digital-to-analog converter (presented next). Note the use of intermediate latches for the converter (even if it includes on-board latches).



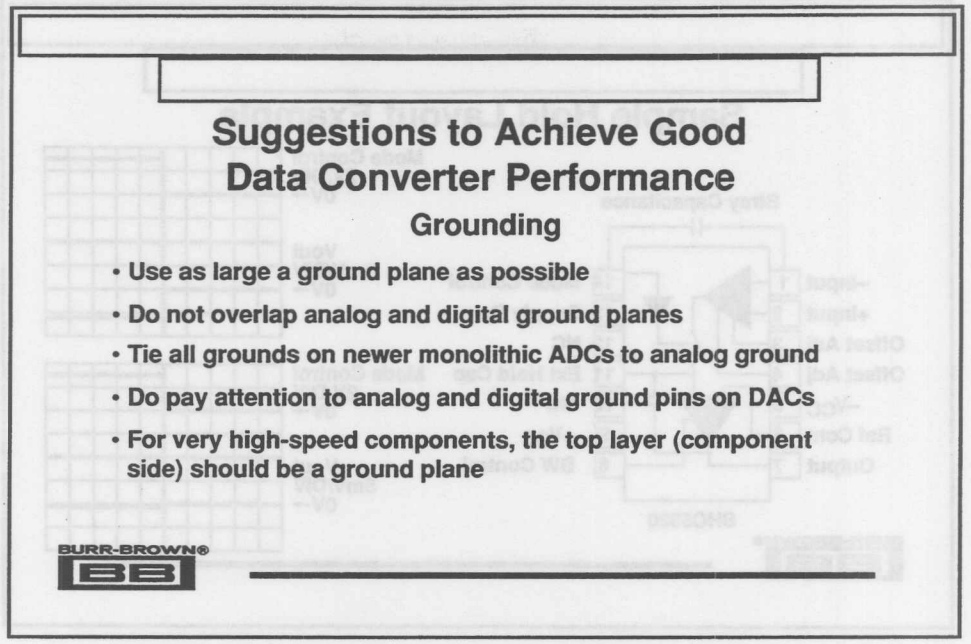
Suggested Layout For Digital-to-Analog Converters

This is the bare essence of laying out a board for modern, monolithic digital-to-analog converters. For high-speed DACs or for designs evolving a great deal of digital logic, a better layout might resemble the layout for an analog-to-digital converter (presented previously). Again, note the use of intermediate latches for the converter (even if it includes on-board latches).



Sample Hold Layout Example

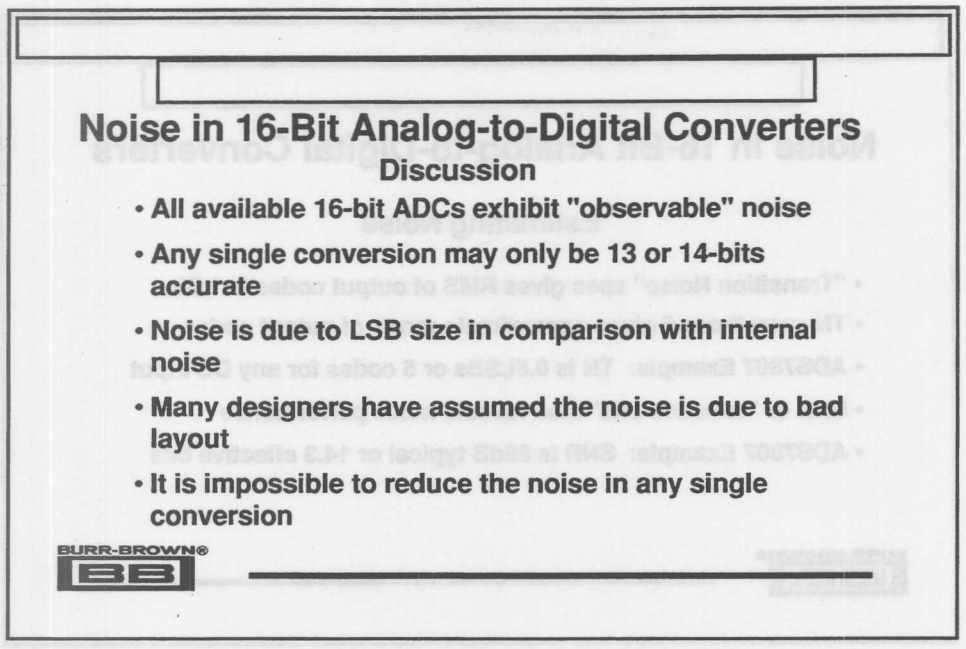
Effects on analog performance from digital signals can be very subtle as this slide shows. Basically, the digital signal on the "Mode Control" pin (pin 14) was coupling into the inverting input (pin1) of the input op-amp. This produced an offset in the output during the hold mode. When the coupling was reduced, the offset was essentially eliminated.



Suggestions to Achieve Good Data Converter Performance

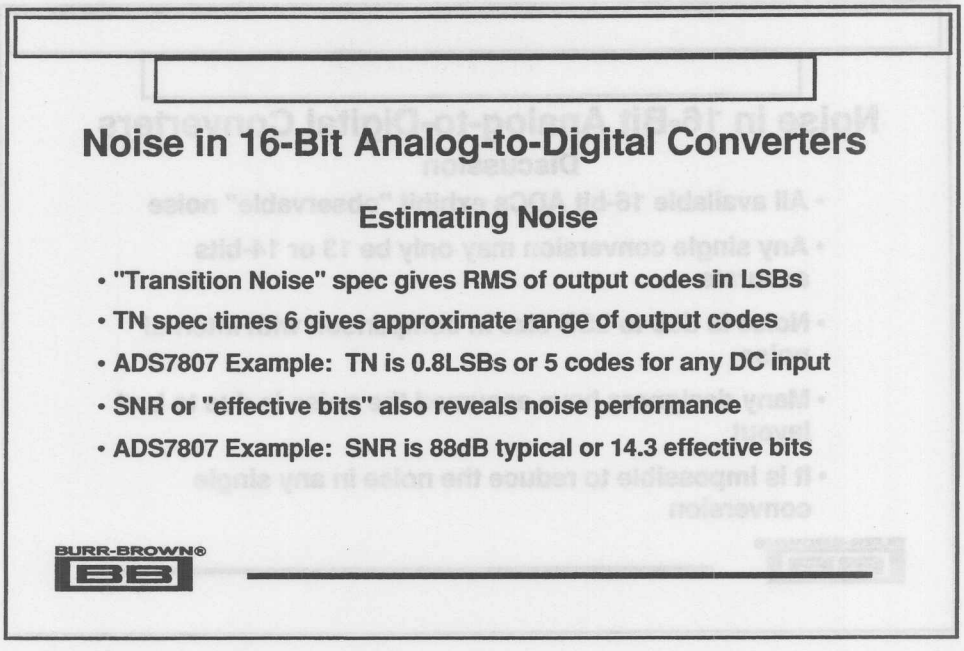
Grounding in any system can be a major problem. This slide does not discuss system grounding at all—many books have been written about this problem alone. This slide concerns grounding a data converter at the "local" level only. Overall, the best rule of thumb is: "Less impedance in the ground plane is better."

Other items on this slide concern where to tie the "analog" and "digital" ground pins on data converters. Here, there are only general guidelines. For newer, "digitally intensive" designs, it's often best to simply put the converter completely on the analog side. However, this may not result in the absolute best performance. Also, digital returns currents can become a problem.



Noise in 16-Bit Analog-to-Digital Converters

The digital output of any 16-bit analog-to-digital converter represents the sum of internal noise and the actual desired conversion. This noise can easily be observed in a series of conversions with a constant DC input voltage—as the output code will vary around the ideal value. The reason is the extremely small size of an "LSB" in relation to the noise inherent in the system. For any single conversion, it is impossible to separate the noise from the actual value.

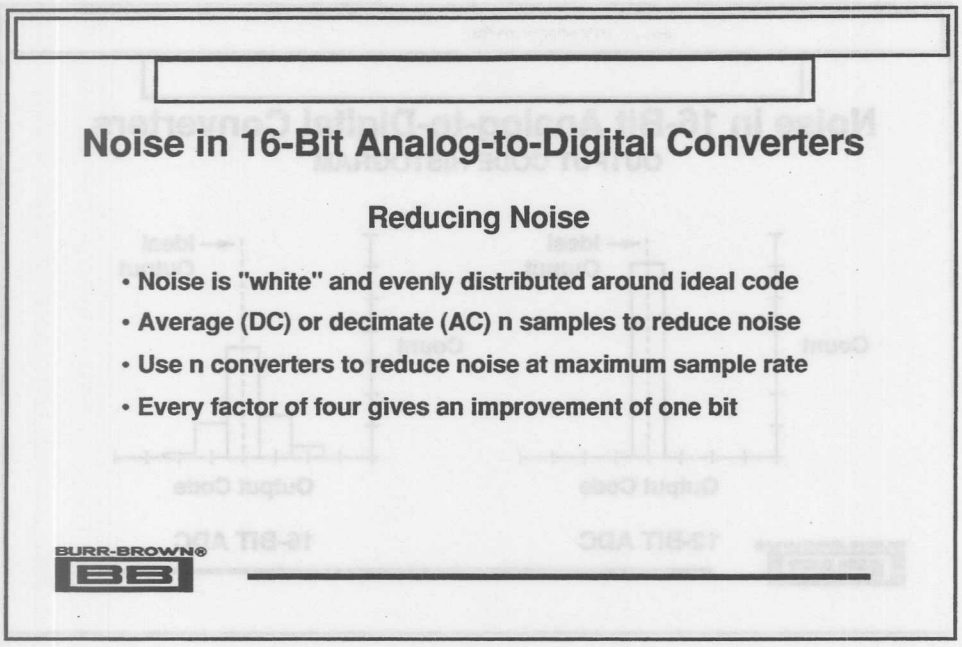


Noise in 16-Bit Analog-to-Digital Converters

Circuit and system designers need to know the extent of noise in an ADC. There are two specifications that can be used to determine this. This best specification is "transition noise." This can essentially be thought of as the standard deviation in output codes from the ideal code—or, as the RMS output codes in LSBs. (Transition noise multiplied by the LSB size is also the RMS noise of the converter.)

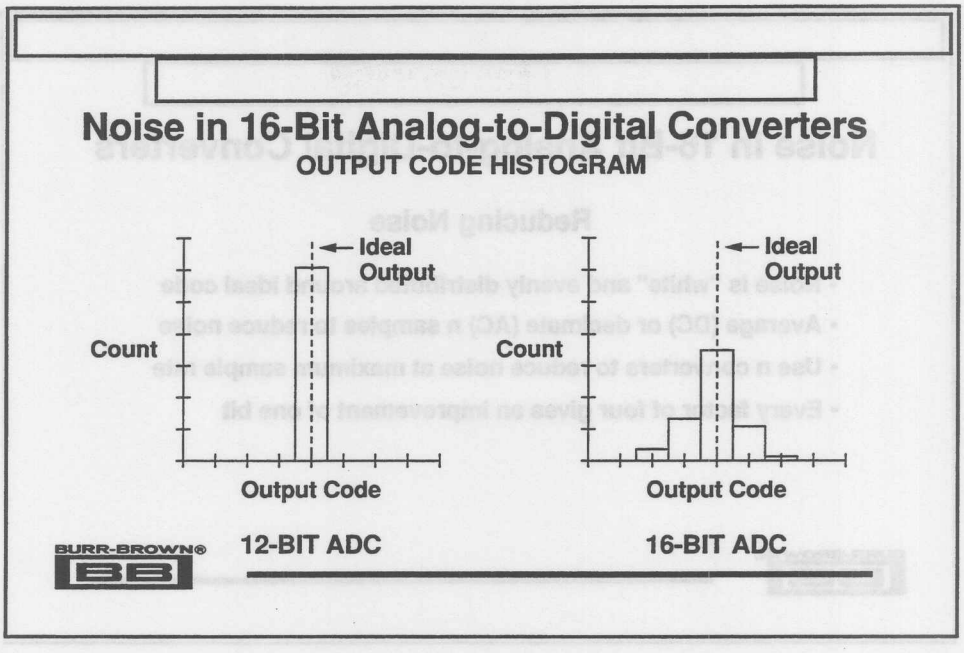
Transition noise multiplied by 6 will yield the approximate range of output codes in a thousand conversions. Obviously, for more conversations, this range will be slightly larger. For an example, the ADS7807 has a transition noise specification of 0.8LSBs.This indicates that a thousand conversions should result in five different output codes. The RMS noise of the converter on a 20V peak-to-peak range is around 250µV.

Another specification which gives an indication of noise performance is signal-to-noise ratio. A true 16-bit converter would have an SNR of 98dB. Real 16-bit converters have SNRs in the 86 to 92dB range. Reversing the calculation would indicate that these converters are 14 to 15-bits accurate for any single conversion.



Noise in 16-Bit Analog-to-Digital Converters

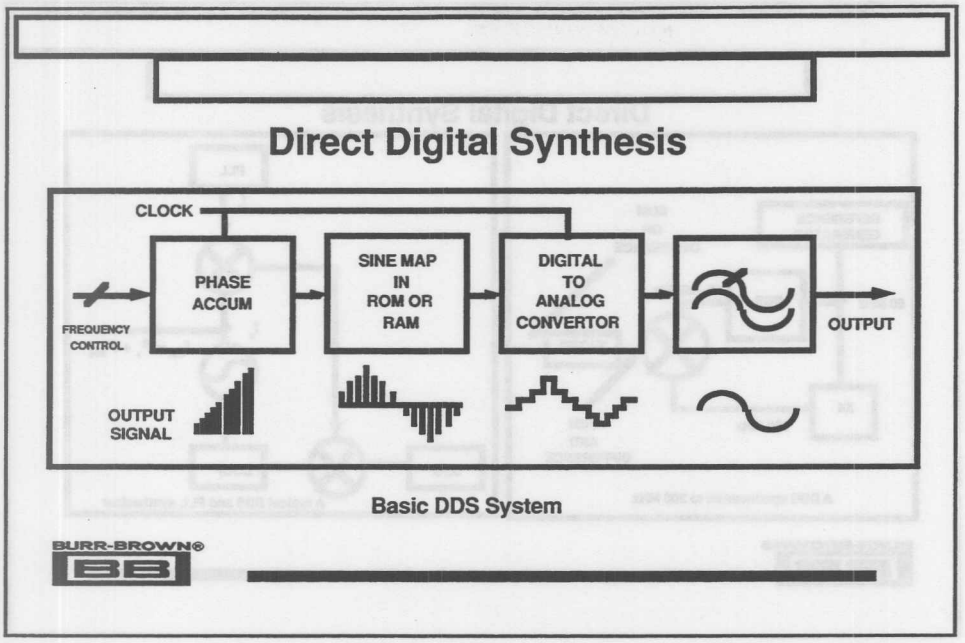
There are several approaches to reducing noise in 16-bit ADCs. All of the methods are based on the statistical nature of the noise, and reduce it through the use of multiple conversions and/or multiple ADCs. By using a single ADC, samples can be averaged but the maximum conversion rate will be reduced. For multiple ADCs, the maximum conversion rate can be maintained but more ADCs are needed. Either way, every factor of four will increase performance by one "effective" bit (with the limit being set by the linearity of the converter).



Noise in 16-Bit Analog-to-Digital Converters

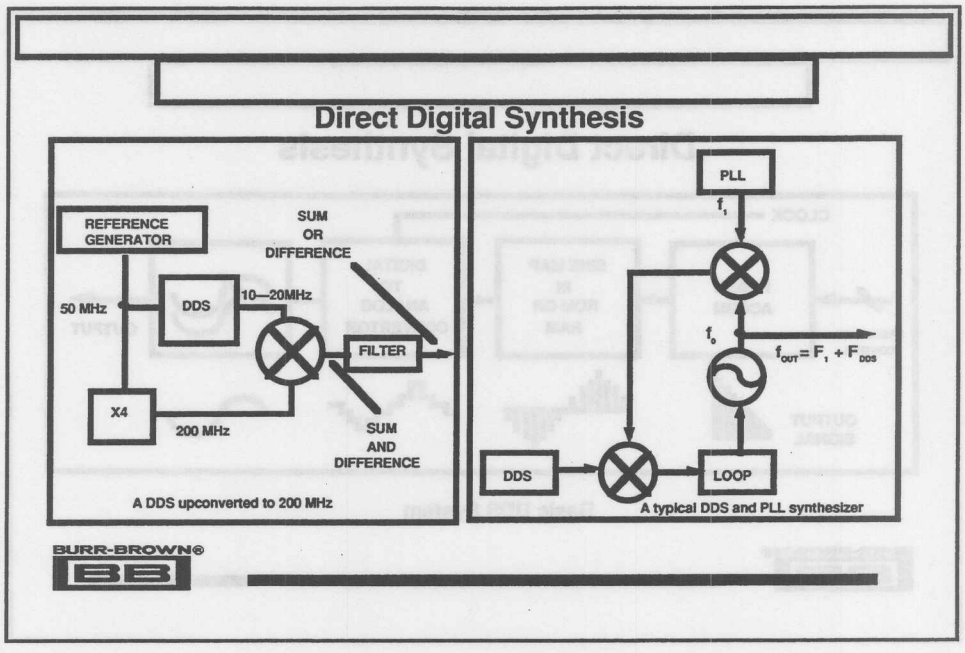
Noise is inherent in all electrical systems. For the most part, the system is either designed to operate far above the noise or operate in a manner where the noise is "tolerated." In a 12-bit analog-to-digital converter, the inherent noise is usually far below the quantization noise. So, it's often easy to place a DC value at the input and see a single, constant output code.

In a 16-bit analog-to-digital converter, this "noise-free" operation is not possible. The inherent noise is actually larger than the quantization noise.



Direct Digital Synthesis

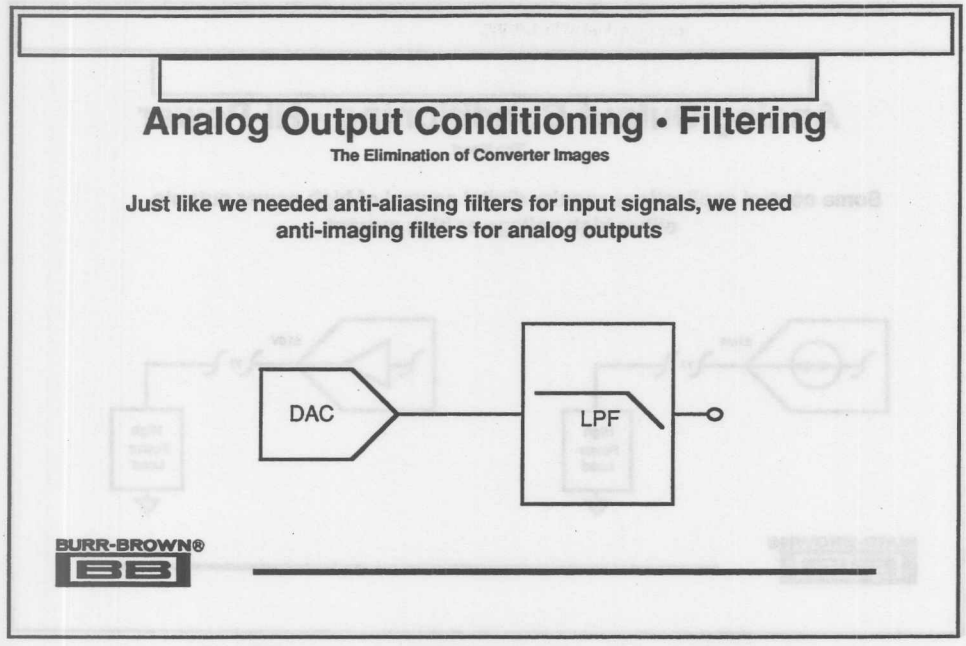
This block diagram represents the basic elements of a Direct Digital Synthesis (DDS) system. The phase accumulator correlates the clock with a control word, defining a ramp from 0° to 360°, which determines the ourput frequency. The sine map ties the phase data to digital amplitude words, so the input to the DAC has both frequency and amplitude. The maximum frequency which can be generated is one half of the clock rate. The useful range of the system, due to spurious components, is typically one-fourth the clock speed or less.



Direct Digital Synthesis

If the system requires high resolution over a narrow band at a relatively high center frequency, a DDS can be upconverted to take advantage of DDS properties. In the first figure, a DDS with relatively low output frequency is mixed with an upconverted sine wave. The DDS can then be used to control fine steps around the center frequency of 200MHz.

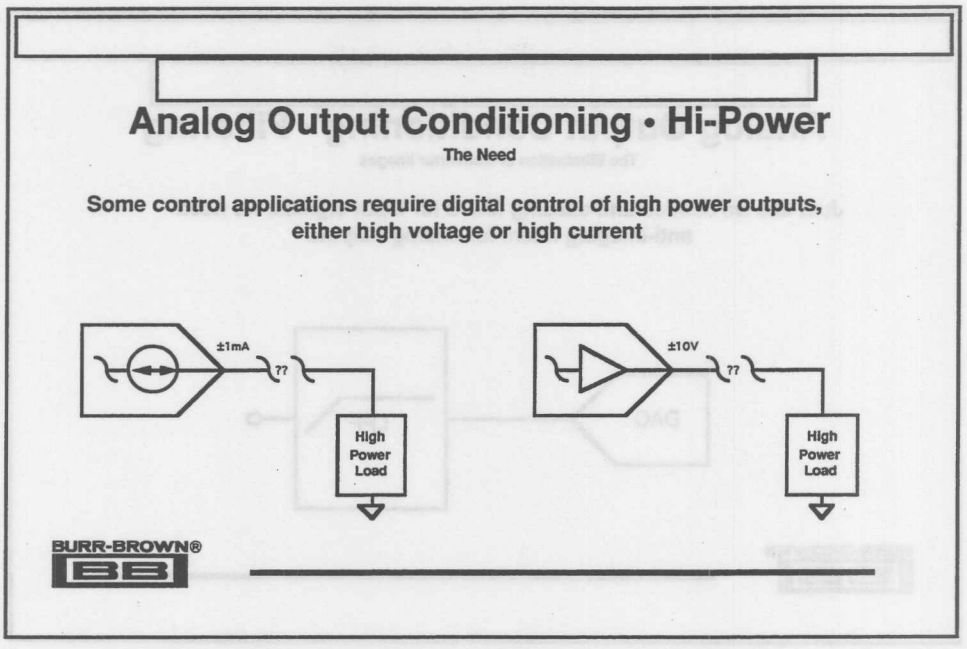
The second figure shows a hybrid system, consisting of a DDS and an analog phase-locked-loop. In this system, the DDS output is mixed with the PLL output, which allows for faster and more accurate tuning than is normally available with an analog PLL.



Analog Output Conditioning • Filtering

The Elimination of Converter Images

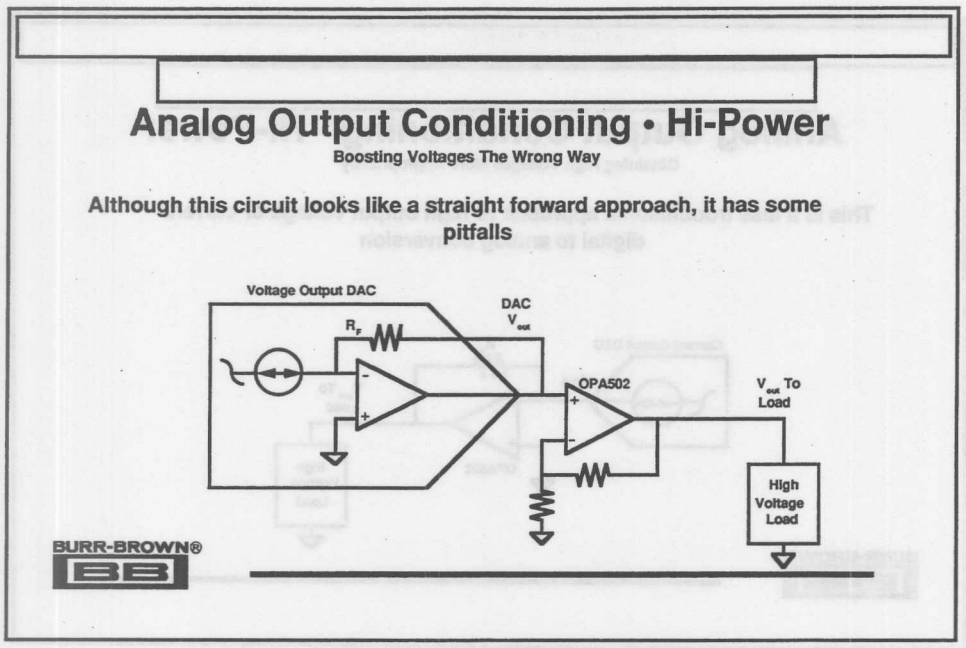
Similar to when the ADC's conversion rate would alias into the analog signal, the DAC's update rate will appear as an "image" in the analog output. Low pass filters can be used to remove this image, as well as any glitch which may be in the DAC's output. For more information on analog filtering, see the "Analog Input Signal Conditioning • Filtering" section of this material.



Analog Output Conditioning • Hi-Power

The Need

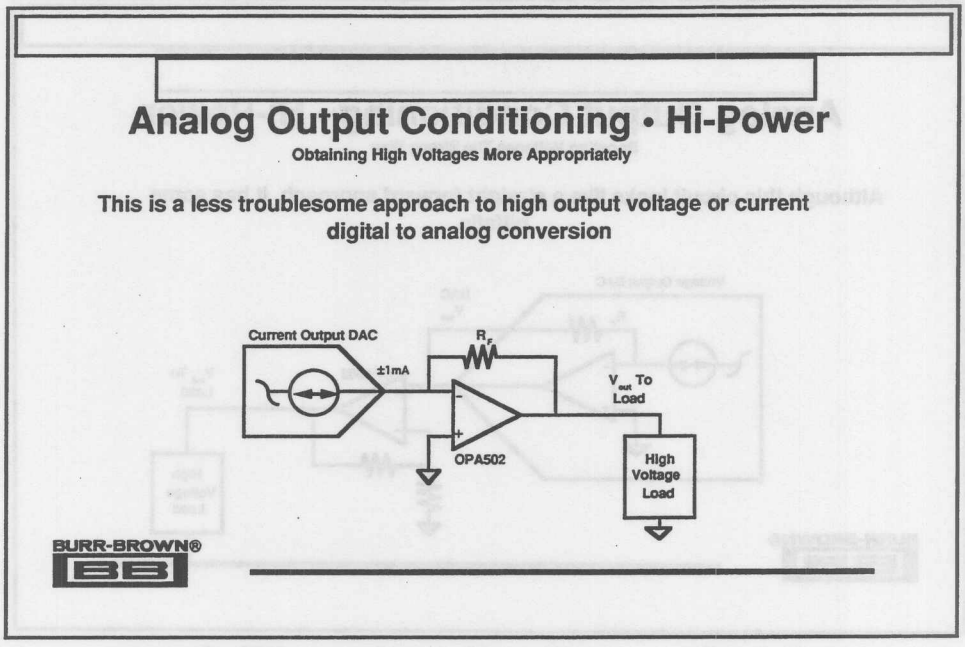
In addition to DDS and arbitrary waveform generation, DACs are also used in a lot of control applications. The typical current output DAC is usually capable of driving up to 2mA, and voltage output DACs are rarely capable of delivering more than ±10V. If you need more output current or voltage than this, some type of "power booster" will be required.



Analog Output Conditioning • Hi-Power

Boosting Voltages The Wrong Way

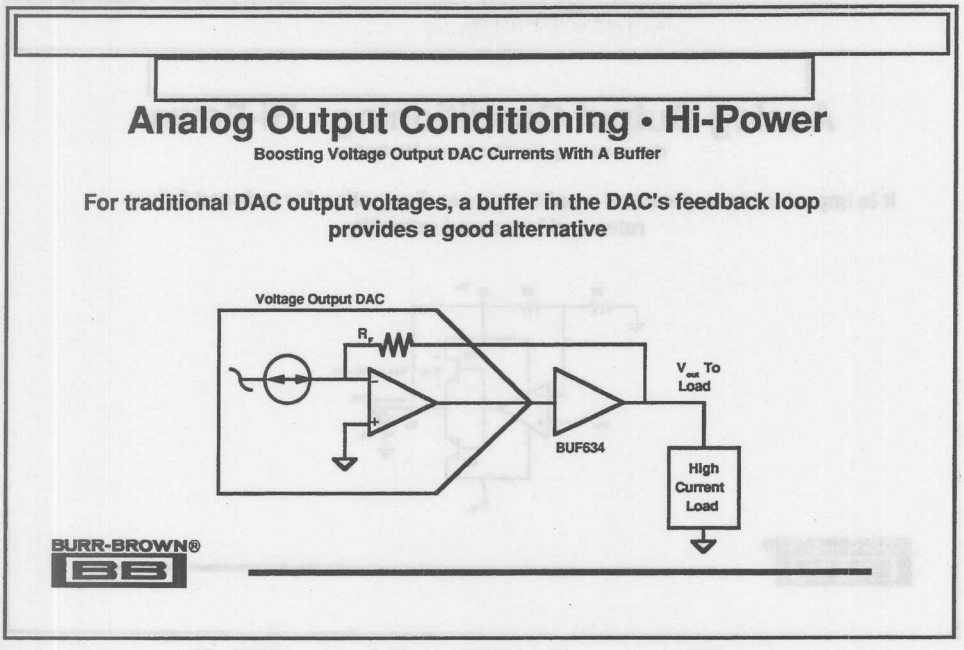
This is probably the circuit configuration that would come to mind initially. The output from a voltage output DAC would simply be multiplied by the gain of the power amplifier circuit. However, now there are two separate analog sources for error - the DAC's op amp and the power amp. Any offset from the DAC's amplifier will be summed with the input offset of the power amplifier and then multiplied by the gain of the power amplifier. There are also two additional resistors whose temperature effects will cause drift in the system.



Analog Output Conditioning • Hi-Power

Obtaining High Voltages More Appropriately

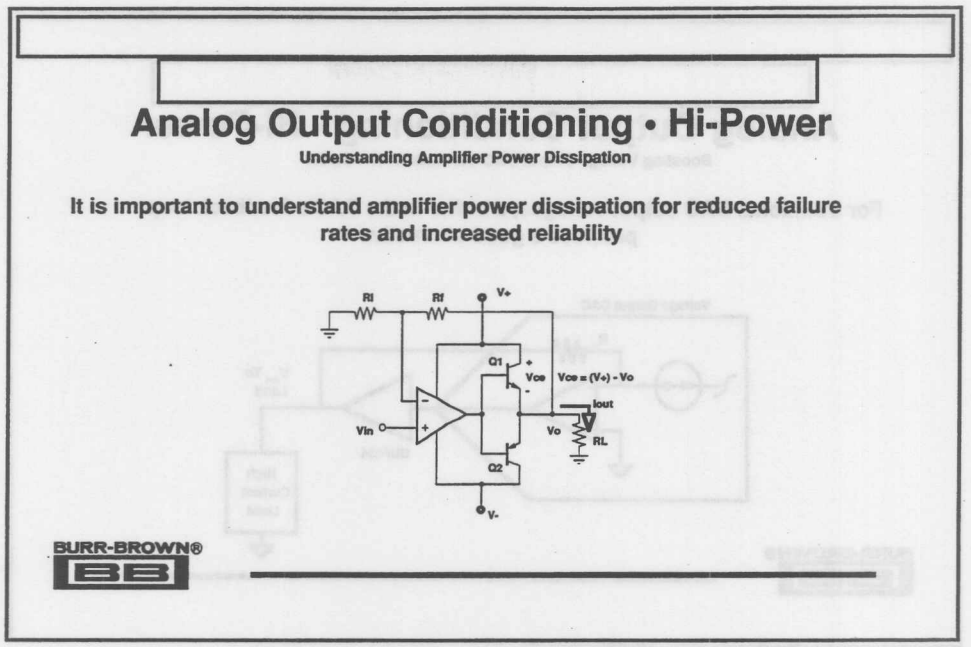
A more appropriate implementation of a high output voltage DAC system uses a current output DAC driving a transimpedance style current to voltage converter (remember, Vout is the product of the input current and the feedback resistor). The amplifier used here might be capable of high voltages, high currents, or both. In this topology, there is only one source of offset voltage error and only one resistor to drift. The transimpedance gain is typically greater than the voltage gain of a transimpedance amplifier, so offset voltage is usually "gained up" by less than the input current. By using the OPA502, output voltages of up to ±35V at ±10A are possible with just about any "garden variety", current output DAC.



Analog Output Conditioning • Hi-Power

Boosting Voltage Output DAC Currents With A Buffer

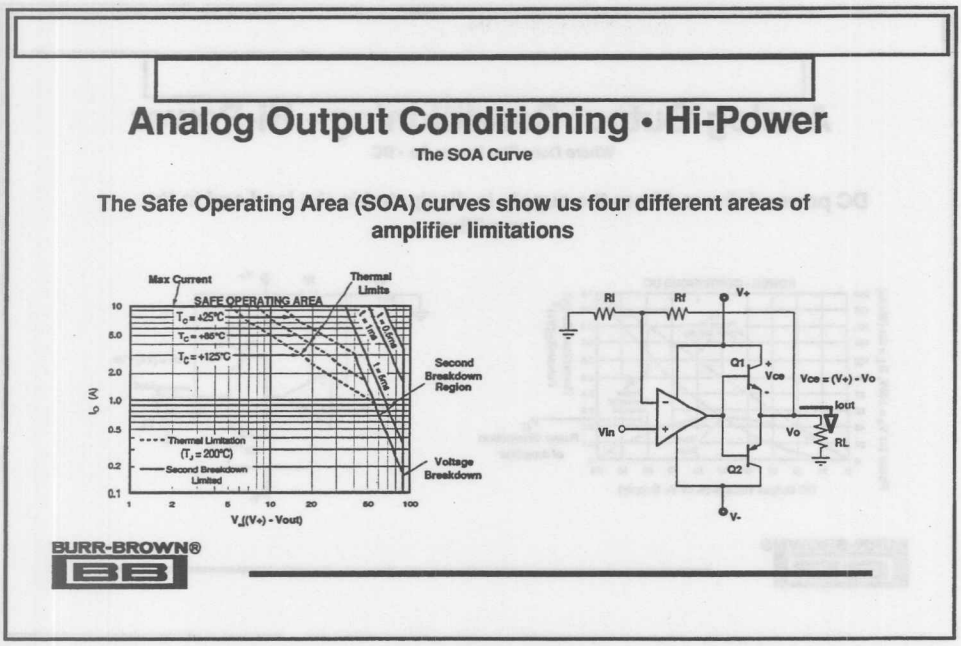
If traditional DAC outputs of ±10V or less are acceptable, but you just need more drive current, consider placing a unity gain buffer amplifier within a voltage output DAC's internal transimpedance network. Using this configuration, as long as the buffer is fast enough to not introduce significant phase shift, the DAC's internal amplifier will control all errors. This includes compensation for any gain error or offset voltage associated with the buffer. Using the BUF634 in the output of a DAC813 makes outputs of ±10V at ±250mA (2.5W) possible.



Analog Output Conditioning • Hi-Power

Understanding Amplifier Power Dissipation

Shown here is a simplified diagram of a power op amp driving a load, R_L. The output transistors Q_1 & Q_2 provide positive and negative load currents respectively. As I_{out} is shown flowing out of the amplifier circuit, Q_1 is conducting and Q_2 is "off", and will be ignored. The amount of power being dissipated in Q_1 is a function of the current flowing through it and the voltage across it (V_{ce}). For a non-reactive load, these values are easily determined. The voltage across Q_1 is V_+ (power supply voltage) minus V_{out}. The current flowing through Q_1 is I_{out}. Therefore, the power being dissipated by Q_1 here is: $P_{Q1} = (I_{out})\bullet(V_+ - V_{out})$. This is one of four important factors in determining whether you are operating an amplifier in its Safe Operating Area (SOA).



Analog Output Conditioning • Hi-Power

The SOA Curve

The SOA graph, using the output stage V_{ce} and I_{out} for the x & y axis respectively, characterizes an amplifier's power handling capabilities. The maximum output current is a function of V_{ce}. The graph has four distinct regions which we will discuss.

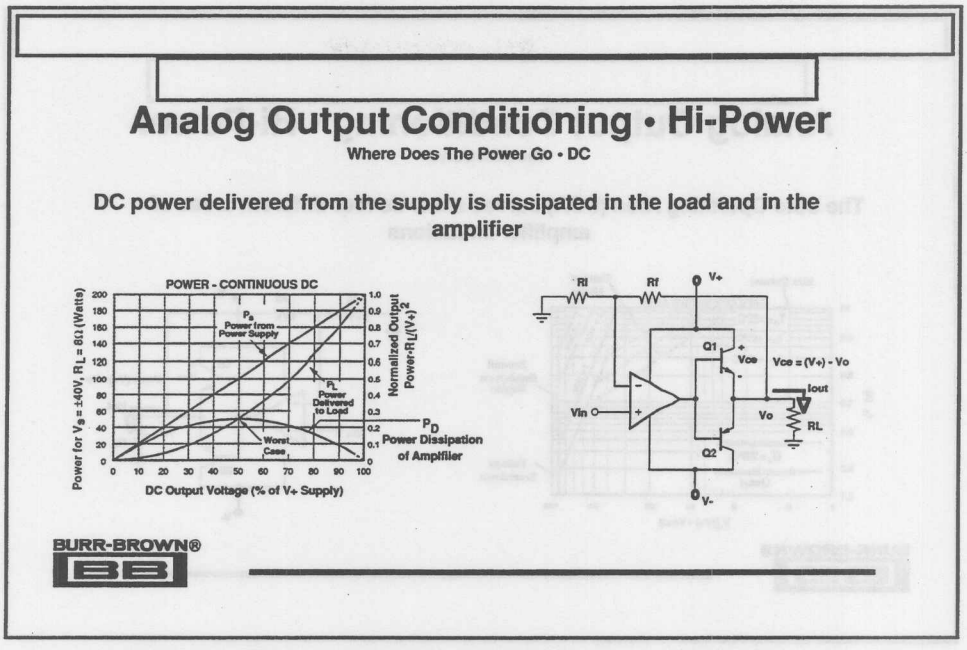
Max Current • At low values of V_{ce}, the amplifier's maximum output current can be delivered. Exceeding the maximum specified current can over stress wire bonds or metallization on the die, causing device failure.

Thermal Limits • At higher values of V_{ce}, the power being dissipated in the output stage transistor causes self heating. This area of the graph indicates the power which raises the temperature of the device to its maximum rated value. All points along these lines produce a constant power dissipation (120W @ 25°C here). Exceeding indicated output in this region may damage, catastrophic or parametric, the output transistor.

Second Breakdown • As V_{ce} is increased further, the safe output current decreases more rapidly. This secondary breakdown region is a function of bipolar transistors. It is caused by the tendency of bipolar transistors to produce points on the transistor where current flow concentrates at high values of V_{ce}. Exceeding the maximum output current in this region produces thermal runaway, causing device failure.

Voltage Breakdown • The vertical line indicates the breakdown voltage of the transistor. Exceeding this voltage can cause device failure.

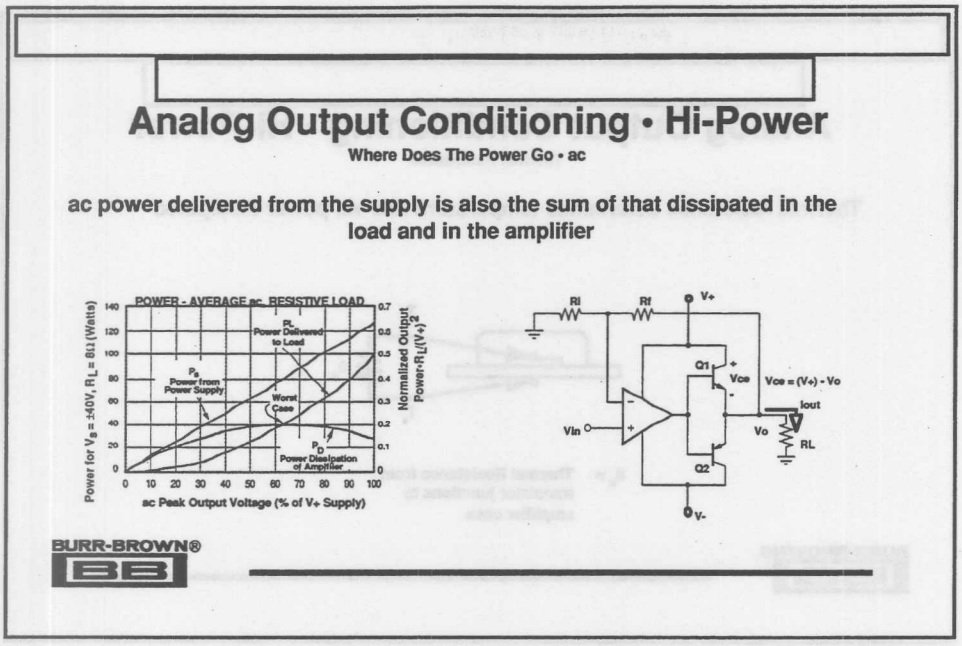
Only resistive load.



Analog Output Conditioning • Hi-Power

Where Does The Power Go • DC

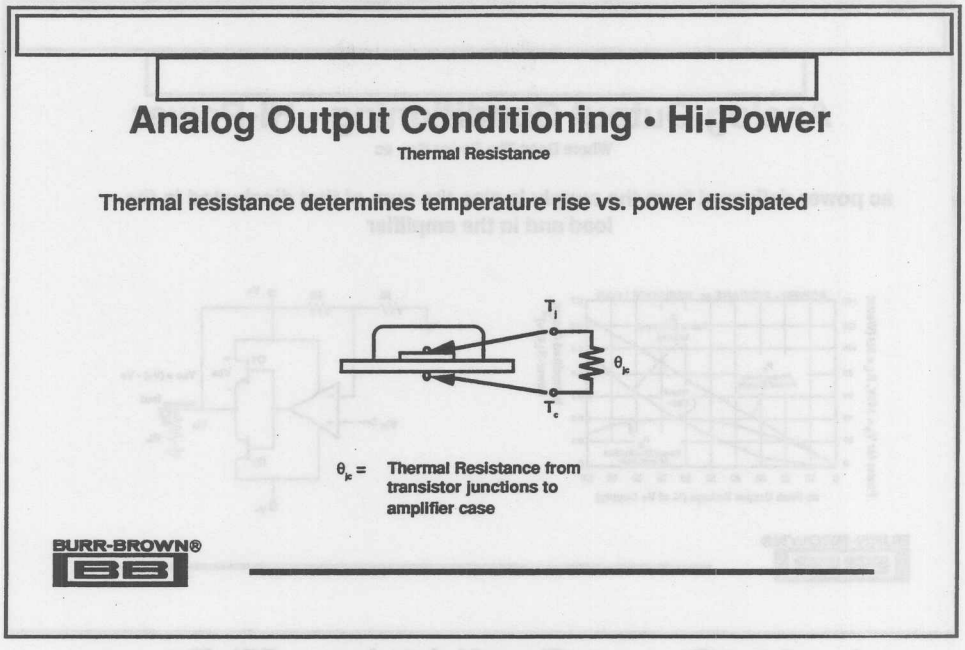
This figure shows three different power versus output voltage curves for a DC resistive load circuit. The straight plot is the power delivered from the power supply. This is simply $(V_+)\bullet(I_{out})$, and is linear in nature. The curve with both inputs the same as the power supply is the power delivered to the resistive load. This is a nonlinear function because as the voltage to a resistive load increases, so does the current (remember, $P=I^2R$). The third curve is the power dissipated in the output transistor. This is simply the power that the supply is delivering minus the power in the load. Notice that the most stressful condition for the transistor occurs at $V_+/2$. The same is true of circuits using unbalanced supplies. For a system using +70V and -5V power supplies, the maximum power in the transistor would occur at V_{out} = +35V. This figure is only valid for DC signals driving resistive loads. Now for ac signals, imagine a signal which rapidly traverses the curves. The maximum transistor power point is passed only briefly. If the ac signal is fast enough (above 50Hz), the thermal time constant of the device causes the transistor temperature to be determined by the average power dissipation. These applications are typically less demanding than DC.



Analog Output Conditioning • Hi-Power

Where Does The Power Go • ac

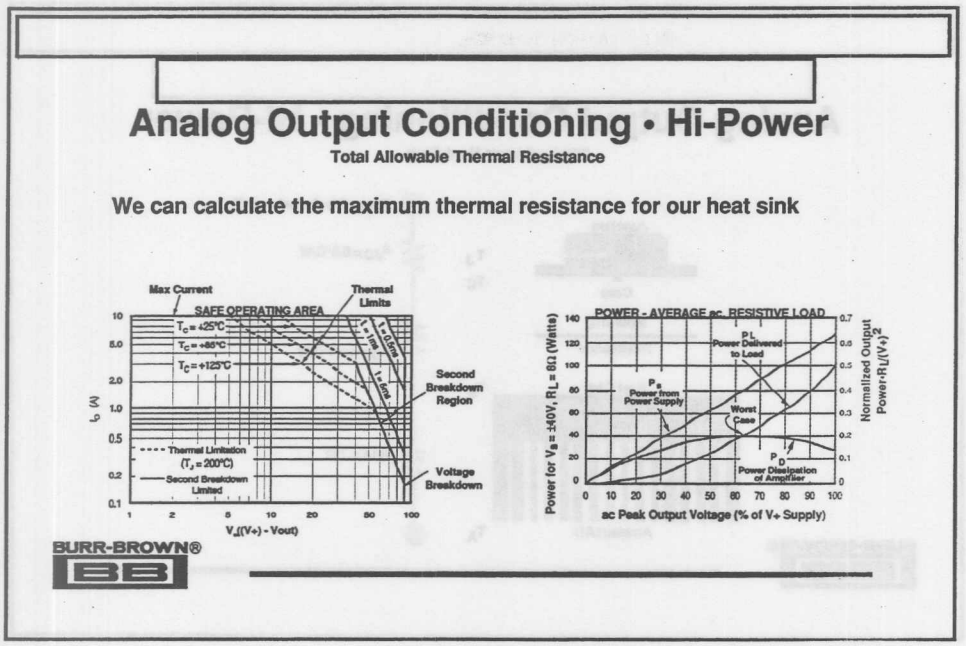
For the first time, we will consider the output current to be bipolar. If centered around zero, each transistor is off for half a cycle and the total amplifier dissipation is shared between the two output transistors. This lowers the effective thermal resistance of the amplifier. This ac power plot once again shows the power delivered from the power supply to a resistive load and the amplifier. This time, the output voltage is the peak voltage of a sinusoidal wave. The shape of the amplifier''s dissipation curve is similar to that with DC signals, but it does not return to zero at $V_{out} = V_{+}$. The worst case signal for a sinusoidal output into a resistive load is at V_{pk} of approximately $0.63 \bullet (V_{+})$. Rarely does an ac application have to operate continuously at this worst case dissipation point. An audio amplifier with voice or music typically dissipates much less power. However, since a sinusoidal waveform of any magnitude is possible, this maximum dissipation point is a good starting point for you. For more information regarding power dissipation with complex waveforms and reactive loads, see Burr-Brown Application Bulletin #39 (AB-039) "Power Amplifier Stress & Power Handling Limitations".



Analog Output Conditioning • Hi-Power

Thermal Resistance

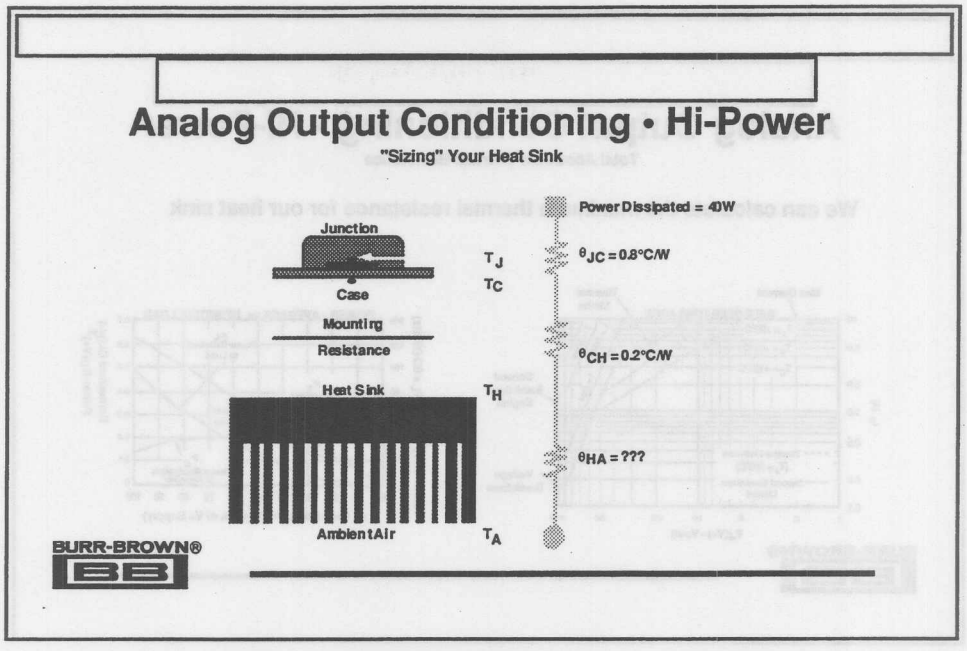
Now that we know about how much power we are dissipating, it's probably time to find a heat sink. The heat sink should be of sufficient size and construction as to keep an amplifier's transistor junctions less than their maximum rated temperature (lower is better). θ is the symbol designated as "thermal resistance", and amplifiers have rated thermal resistances. The OPA502 has an ac θ_{jc} (thermal resistance from transistor junction to amplifier case) of approximately 0.8°C/W. This means that for every watt of power dissipated, the transistor junctions will rise 0.8°C above the amplifier case temperature. If we keep the case at 25°C and dissipate 10W, the amplifier junctions will be at approximately 33°C. The trouble is keeping the case at 25°C.



Analog Output Conditioning • Hi-Power

Total Allowable Thermal Resistance

Using the SOA curves for the OPA502 power op amp and the power curves we referred to earlier for ac applications, we will determine the maximum thermal resistance we require of a heat sink. We need to determine maximum ambient temperature - let's pick 25°C. According to the SOA, we can dissipate 120W at a 25°C case temperature, but we're only going to use 40W according to our power plot. Using a maximum junction temperature of 150°C, the junction can rise 125°C above ambient. The overall thermal resistance from junction to ambient should be no more than 125°C/40W = 3.125°C/W.



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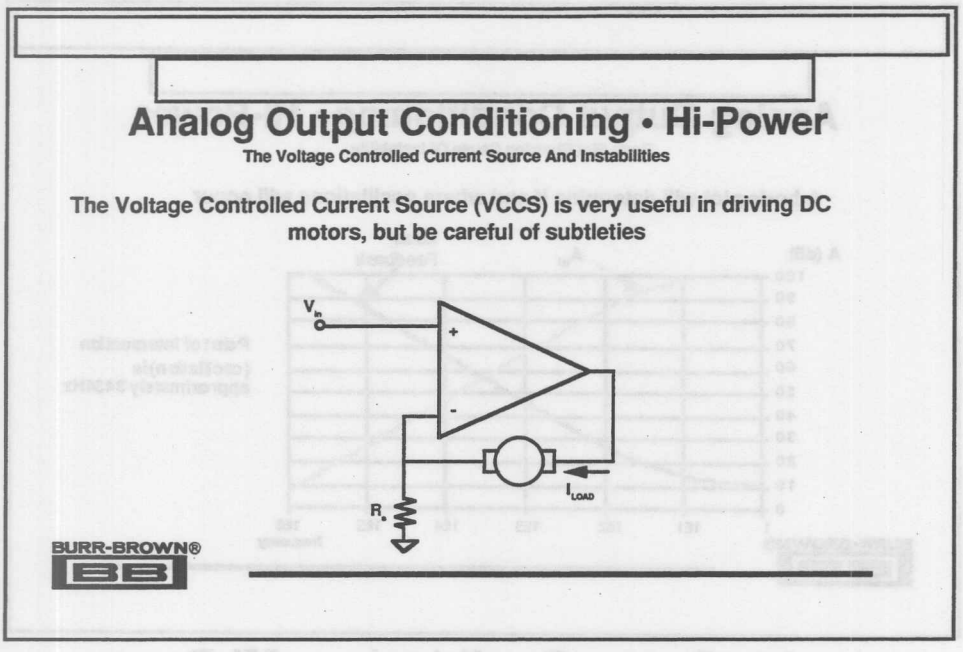
"Sizing" Your Heat Sink

This figure shows the various thermal resistances associated with mounting an amplifier package. Just like the amplifier has a thermal resistance from transistor junction to its case, a heat sink also has a thermal resistance from its case to the ambient, θ_{HA}. There is also a thermal resistance associated with mounting the amplifier to the heat sink, θ_{CH}. The sum of all three of these thermal resistances must be less than 3.125°C/W for our circuit, and 0.8°C/W is already defined as θ_{JC}. The sum of θ_{CH} and θ_{HA} must be less than 2.325°C/W. By using the Q2-88 (with 0.094" holes) from Bergquist you can achieve a θ_{CH} of about 0.2 °C/W. Therefore, we will need a heat sink with a thermal resistance of ≤2.125°C/W.

no thermal compound.



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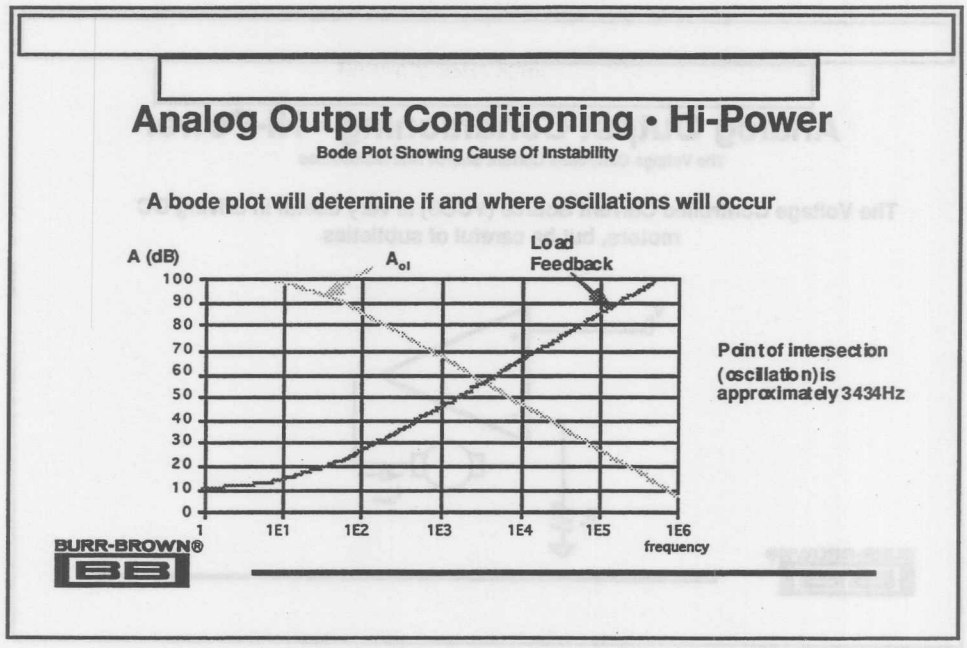
The Voltage Controlled Current Source And Instabilities

In many applications of power amplifiers, a voltage needs to be converted to a current. This figure shows the most common circuit for this transformation. The op amp is connected as a voltage controlled current source with the load contained within the op amp's feedback loop. Since an op amp keeps the voltage at its summing junction the same as the voltage on the non-inverting input, the load current is simply V_{in}/R_s (with the exception of offset voltage). However, when driving inductive loads such as DC motors (motor torque is directly proportional to the current through it), there are some subtleties which can really plague you...



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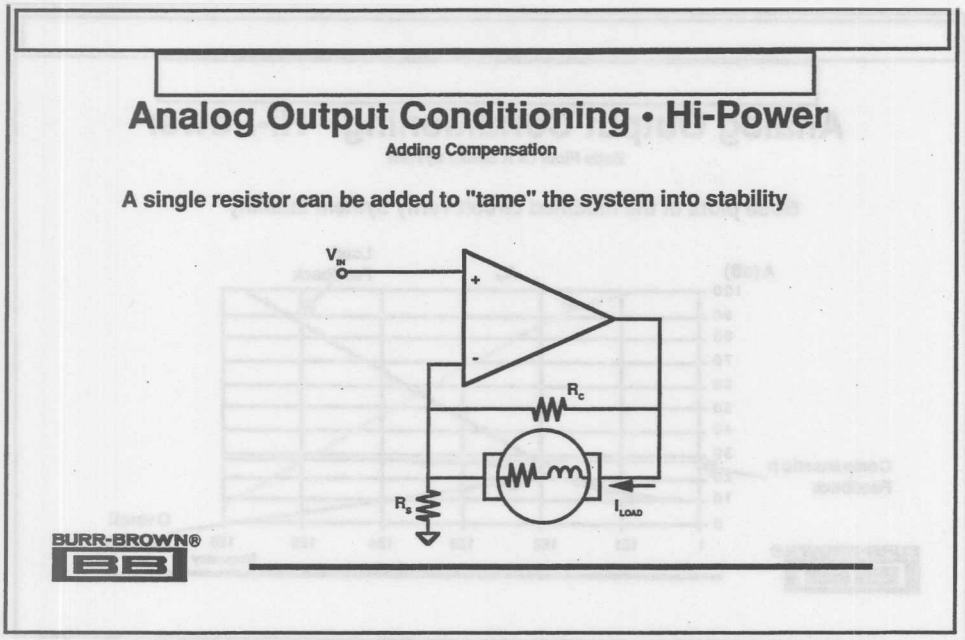
Bode Plot Showing Cause Of Instability

The inductance of the motor windings causes the feedback impedance to be frequency dependent. Shown here is the open loop gain curve (A_{ol}) for the OPA502 and the closed loop gain curve which is a factor of the motor inductance and resistance, and the sense resistor R_s. Since the open loop gain is falling at 20dB/decade and the closed loop gain is rising at 20dB per decade, instability results. This particular circuit should oscillate at approximately 3434Hz, or where the two curves intersect. Don't worry, this can be "compensated" for. The corner frequency in the closed loop gain curve is equal to: $(R_L + R_s)/2\pi L_L$. All we need to do is to introduce an element which will "tame" this frequency dependent gain.

Could use to find L of motor.



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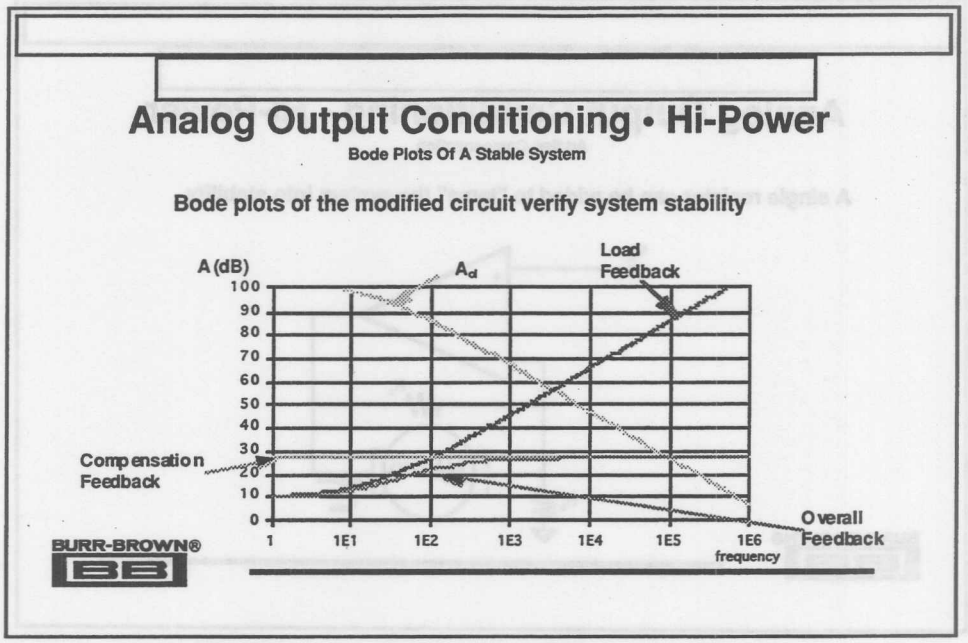
Adding Compensation

We typically think of needing reactive elements (mainly capacitors) to provide compensation, but all that is needed here is a resistance, R_c, which will dictate high frequency feedback. As the motor's inductive reactance rises above about 10Ω, the parallel equivalent impedance of the two feedback networks asymptotically approaches the gain achieved with just the compensation resistance.



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Bode Plots Of A Stable System

This bode plot has the same information as the previous one, but two additional curves have been added. The "Compensation Feedback" curve shows the gain vs. frequency of the resistor added (arbitrarily chosen to be 10x the value of the motor's DC resistance), which is flat with respect to frequency. The other curve (Overall Feedback) shows the overall closed loop gain when both the motor and compensation resistor are used. Notice that the point of intersection is now a "calm" 20dB/decade, which indicates stability. Although motor inductances are not usually specified by motor manufacturers, an empirical approach can be used in determining the amount of compensation resistance to be used.